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# Sequential Afterglow Processing and Non-Contact Corona-Kelvin Metrology of 4H-SiC

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# Sequential Afterglow Processing and Non-Contact Corona-Kelvin Metrology of 4H-SiC

by

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ABSTRACT

Silicon carbide (SiC) is a wide band-gap semiconductor with advantageous electrical and thermal properties making it attractive for high temperature and power applications. However, difficulties with oxide/SiC structures have posed challenges to the development of practical MOS-type devices. Surface conditioning and oxidation of 4H-SiC were investigated using a novel sequential afterglow processing approach combined with the unique capabilities of non-contact corona-Kelvin metrology. The use of remote plasma assisted thermal oxidation facilitated film growth at low temperature and pressure with the flexibility of sequential *in-situ* processing options including pre-oxidation surface conditioning. Corona-Kelvin metrology (C-KM) provided a fast, non-destructive method for electrical evaluation of oxide films and semiconductor surfaces. Non-contact C-KM oxide capacitance-voltage characteristics combined with direct measurement of SiC surfaces using C-KM depletion surface barrier monitoring and XPS analysis of surface chemistry were interpreted relating the impact of afterglow conditioning on the surface and its influence on subsequent oxide thin film growth. Afterglow oxide films of thicknesses 50–500 Å were fabricated on SiC epi-layers at low growth temperatures in the range 600–850°C, an achievement not possible using conventional atmospheric oxidation techniques. The inclusion of pre-oxidation surface conditioning in forming gas ($N_2$:$H_2$)* afterglow was found to produce an increase in

oxide growth rate (10–25%) and a significant improvement in oxide film thickness uniformity. Analysis of depletion voltage transients on conditioned SiC surfaces revealed the highest degree of surface passivation, uniformity, and elimination of sources of charge compensation accomplished by the $(N_2:H_2)$* afterglow treatment for 20 min. at 600–700°C compared to other conditioning variations. The state of surface passivation was determined to be very stable and resilient when exposed to a variety of temporal, electrical, and thermal stresses. Surface chemistry analysis by XPS gave evidence of nitrogen incorporation and a reduction of the C/Si ratio achieved by the $(N_2:H_2)$* afterglow surface treatment, which was tied to the improvements in passivation, uniformity, and growth rate observed by non-contact C-KM measurements. Collective results were used to suggest a clean, uniform, passivated, Si-enriched surface created by afterglow conditioning of 4H-SiC as a sequential preparation step for subsequent oxidation or dielectric formation processing.

# Chapter 1. Introduction and Background

Single-crystal silicon carbide (SiC) is a promising wide band-gap (WBG) semiconductor material for future power electronic device applications, but requires continued technological improvement in order to realize practical metal-oxide-semiconductor field-effect transistor (MOSFET) devices. SiC possesses superior electrical and thermal properties compared to silicon (Si), while remaining one of the few semiconductor materials forming silicon dioxide ($SiO_2$) as its native oxide. This allows thermal oxidation methods to be employed in the fabrication of MOSFET power devices. The 4H hexagonal form of SiC has great potential due to its wider band-gap and large electron mobility compared to other commonly investigated SiC polytypes. However, electrically active defects present in the $SiO_2$/4H-SiC material system have drastically limited achievable channel carrier mobilities and threshold voltage stability in device research efforts to date.

Remote plasma assisted thermal processing offers an advantageous and flexible alternative to the conventional atmospheric thermal oxidation approach. An afterglow chemical reactor is capable of forming oxide films on SiC at higher growth rates and at temperatures hundreds of degrees lower than required in traditional atmospheric oxidation furnace processes. Oxide growth at lower furnace temperatures is attractive for several reasons including lower processing cost. Atomic and excited oxidant species generated in a plasma discharge are suspected to play critical roles in oxidizing reactions

at the interface. Furthermore, oxidation by the afterglow method lends itself to the power and flexibility of sequential *in-situ* processing, including pre-oxidation surface conditioning steps and post-oxidation anneals in specific and novel chemical environments.

Electrical measurements of semiconductor and oxide characteristics are critical to the development of any material process or device application requiring dielectric films and interfaces. In-line metrology provides significant advantages over other common measurement techniques requiring additional device fabrication or thin film application. The ability to perform electrical measurements without building test structures translates to immense savings in time and cost of production. In addition, a non-contact characterization technique capable of obtaining quick, non-destructive electrical measurements gives one the opportunity to strategically implement this metrology at selected points in a sequence of processes.

This work entails an investigation of $SiO_2$/4H-SiC structures by applying the unique capabilities of remote plasma afterglow thermal processing and non-contact metrology to the growth and characterization of oxide thin films on 4H-SiC, with a focus on the impact of pre-oxidation surface conditioning.

## 1.1. SiC material properties and device applications

Silicon carbide is a binary compound semiconductor material comprised of Si and carbon (C) covalently bonded in a crystalline lattice. The tetrahedral bonding arrangement depicted in figure 1.1 is the building block of every SiC crystal, with C-Si bond lengths measuring 1.89 Å and adjacent C atoms separated by 3.08 Å. The SiC lattice is structured with alternating planes of Si and C atoms. Each of the 170 polytypes

of SiC is defined by its specific ordering of atomic bi-layers of Si and C planes. The SiC polytype nomenclature contains a number referring to the amount of bi-layers after which the stacking order repeats. Among the most commonly investigated forms of SiC are the 3C, 4H, and 6H-SiC polytypes, with bi-layer stacking sequences of ABCABCA..., ABCBABCBA..., and ABCACBABCACBA..., respectively. The C or H polytype suffixes refer to the cubic or hexagonal crystal structure of the unit cell.

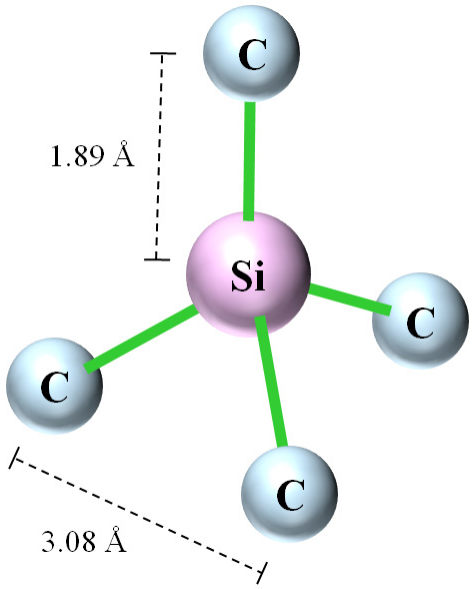


Figure 1.1. Tetrahedral bonding arrangement found in a SiC crystalline lattice.

SiC materials possess a wide energy band-gap ($E_g$), high thermal conductivity ($K$), large breakdown voltage ($V_{BD}$), extremely low intrinsic carrier concentration ($n_i$), and chemical inertness. The aforementioned properties are well-suited for electronic device applications requiring high power, high voltage, and high frequency operation in high-temperature and corrosive environments. The 4H-SiC polytype has generated the most research interest due to its wider band-gap and large electron mobility compared to other commonly investigated SiC polytypes. Table 1.1 lists selected semiconductor material

parameters of several SiC polytypes as well as Si. Note that 4H-SiC possesses 3× larger $E_g$ than Si, and 19 orders of magnitude smaller $n_i$ than Si.

Table 1.1. Selected material properties of SiC and Si semiconductors at 27°C. Note that 4H-SiC has 3× larger energy band-gap and 19 orders of magnitude smaller intrinsic carrrier concentration compared to Si.

| | 4H-SiC | 6H-SiC | 3C-SiC | Si |
|---|---|---|---|---|
| $E_g$ (eV) | 3.26 | 3.03 | 2.36 | 1.12 |
| $n_i$ ($cm^{-3}$) | $5 \times 10^{-9}$ | $1.6 \times 10^{-6}$ | $1.5 \times 10^{-1}$ | $1.45 \times 10^{10}$ |
| $\mu_n$ @ $N_d = 10^{16}$ $cm^{-3}$ ($cm^2$ $V^{-1}$ $s^{-1}$) | 800 | 400 | 800 | 1430 |
| $V_{SAT}$ (cm $s^{-1}$) | $2.5 \times 10^7$ | $2 \times 10^7$ | $2.5 \times 10^7$ | $1 \times 10^7$ |
| $V_{BD}$ @ $N_d = 10^{17}$ $cm^{-3}$ (MV $cm^{-1}$) | 3 | 3.2 | 1.5 | 0.3 |
| $K$ (W $cm^{-1}$ $K^{-1}$) | 4.9 | 4.9 | 3.2 | 1.31 |
| $\varepsilon_r$ | 9.66 | 9.7 | 9.72 | 11.9 |

SiC is particularly appealing for MOSFET power device applications because it is one of the few semiconductors which form a native $SiO_2$ oxide layer, this due to the presence of Si in the crystal lattice. Because of this important property, numerous attempts have been made to apply thermal $SiO_2$ growth techniques to SiC materials, analogous to the $SiO_2$/Si based technology which has achieved unequaled success. However, practical SiC-based devices to date have been junction-type, as MOS structures of desired quality have not been realized. A number of challenging problems have contributed to this failure, some of which are linked to the SiC material quality itself. Bulk crystal quality is poor since substrates are produced by a sublimation process at very high temperatures with high metal contamination levels. Furthermore, growth of high-

quality defect-free epitaxial films critical for device applications has not been achieved. Epitaxial processes either generate or propagate defects from the substrate, resulting in a relatively low quality of starting material for oxidation.

## 1.2. Theory of oxidation

Perhaps the most promising advantage that SiC holds over other WBG materials is its ability, like Si, to thermally oxidize to form $SiO_2$. In an attempt to understand and model the SiC oxidation mechanism and kinetics, it is helpful to first consider the relatively simple oxidation of Si [1].

### 1.2.1. Deal Grove linear-parabolic model for thermal oxidation of Si

Oxidation of silicon is governed by the transport of oxidant molecules to the $SiO_2$/Si interface and reaction with Si surface atoms according to the relation

$$Si + O_2 \leftrightarrow SiO_2 \quad (1)$$

Si oxidation proceeds in a three-step sequence:

1) gas-phase transport and adsorption of molecular oxygen to the oxide surface,
2) in-diffusion of oxidant molecules through any existing oxide film,
3) reaction with Si at the buried $SiO_2$/Si interface.

The first step is assumed to be rapid and not rate-controlling. A diagrammatic representation of the various stages involved in the oxidation of Si is depicted in figure 1.2a. The flux of oxidant molecules from the gas phase to the oxide surface is

$$F = h(C^g - C^s) \quad (2)$$

where h is the gas-phase transport coefficient, $C^g$ is the equilibrium concentration of oxygen gas molecules, and $C^s$ is the oxidant molecule concentration at the outer surface

of the existing oxide film. The flux of oxidant molecules diffusing inward through the oxide film is defined as

$$F = D(C^s - C^i) / X \quad (3)$$

where D is the effective diffusion coefficient of oxidant in the oxide film, $C^i$ is the oxidant molecule concentration near the $SiO_2$/Si interface, and X is the thickness of the existing oxide film. Finally, the flux associated with the interfacial oxidation reaction is expressed as

$$F = kC^i \quad (4)$$

where k is the rate constant of the forward reaction (1). The oxide growth rate at the $SiO_2$/Si interface can be described as

$$dX/dt = F/N_0 \quad (5)$$

where $N_0$ is the number of oxidant molecules incorporated into a unit volume of $SiO_2$. The general model for the thermal oxidation of Si developed by Deal and Grove [2] assumed the three series fluxes of oxidant molecules to be constant and identical in steady state condition. Equating oxidant fluxes (2-4) and solving the differential equation (5) with some approximations yields the general quadratic form expressed as

$$X^2 + AX = B(t + \tau) \quad (6)$$

where B and B/A are parabolic and linear rate constants, respectively, t is time of oxidation, and $\tau$ is related to an initial thickness $X = X_i$ assumed at $t = 0$. The rate constants and initial thickness parameter were defined as follows:

$$B \approx 2(C^g/N_0)D \quad (7)$$

$$B/A \approx (C^g/N_0)(k^{-1} + h^{-1})^{-1} \quad (8)$$

$$\tau = (X_i^2 + AX_i) / B \quad (9)$$

For short oxidation times and thin films, the oxidation rate is limited by the reaction at the $SiO_2$/Si interface, and equation (6) can be approximated by

$$X \approx (B/A)(t + \tau) \tag{10}$$

resulting in a linear thickness-time dependence. Alternatively, for long growth times and thick films, the growth rate is controlled by oxidant in-diffusion through the oxide film, and equation (6) reduces to

$$X^2 \approx Bt \tag{11}$$

resulting in a parabolic relation between thickness and growth time.

The Deal Grove linear-parabolic model successfully predicts thermal oxide growth rates on Si over a wide range of temperatures, times and thicknesses. However, for oxidation by $O_2$ molecules in the thin initial growth regime, experimentally observed growth rates and thicknesses are consistently higher than predicted by the linear-parabolic model.

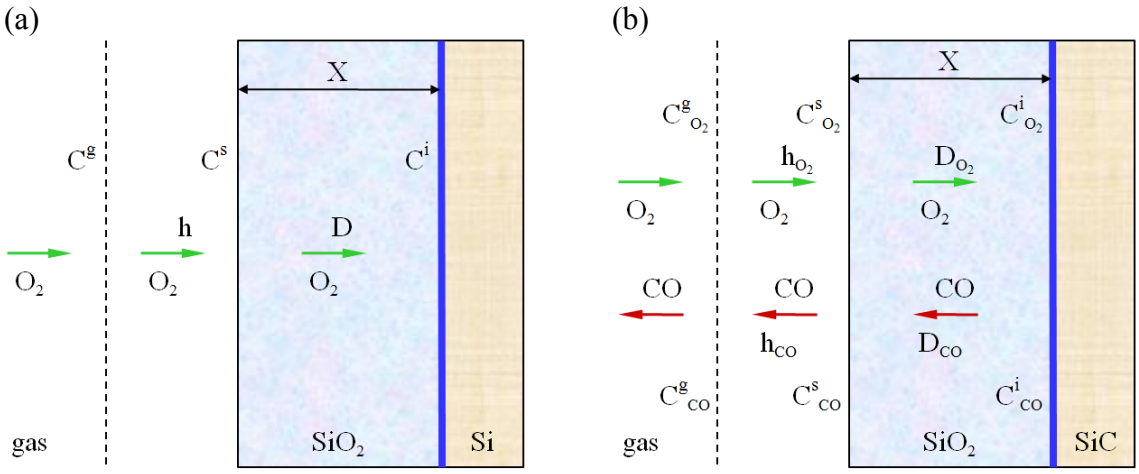


Figure 1.2. Transport steps assumed in modeling thermal oxidation of Si (a) and SiC (b).

### 1.2.2. Model for thermal oxidation of SiC

Oxidation of SiC is somewhat more complex than Si due to the additional role of carbon in the growth kinetics. SiC oxidation is governed by the reaction

$$SiC + 1.5O_2 \leftrightarrow SiO_2 + CO \quad (12)$$

The SiC oxidation process can be described as a sequence of five steps:

1) gas-phase transport of molecular oxygen and adsorption to the oxide surface,
2) in-diffusion of oxidant molecules through the existing oxide film,
3) reaction with Si and C at the buried $SiO_2$/SiC interface,
4) out-diffusion of volatile reaction products (i.e. CO) through the oxide,
5) desorption and removal of CO products to the gas phase,

where the first and last steps are assumed to be fast and not rate-limiting. The last two steps, not present in the oxidation of Si, add complexity to the SiC oxidation mechanism. Figure 1.2b visualizes the transport stages involved in the thermal oxidation of SiC. The Deal Grove model cannot be directly applied to SiC oxidation since it does not account for the out-diffusion and removal of CO products. However, a similar approach has been implemented to examine SiC oxidation kinetics [3]. As before, the steady state in-flux ($F_{O_2}$) of oxidant molecules through the gas phase and $SiO_2$ film is expressed as

$$F_{O_2} = h_{O_2}(C^g_{O_2} - C^s_{O_2}) = D_{O_2}(C^s_{O_2} - C^i_{O_2}) / X \quad (13)$$

Similarly, the steady state flux ($F_{CO}$) describing the out-diffusion and removal of carbon products is

$$F_{CO} = D_{CO}(C^i_{CO} - C^s_{CO}) / X = h_{CO}(C^s_{CO} - C^g_{CO}) \quad (14)$$

where coefficient and concentration subscripts are used to distinguish between $O_2$ and CO molecules. The flux ($F_R$) corresponding to the interfacial oxidation reaction is

$$F_R = k_f C^i_{O_2} - k_r C^i_{CO} \quad (15)$$

where $k_f$ and $k_r$ are the forward and reverse rate constants of the oxidation reaction (12). Again, the growth rate of the $SiO_2$ layer is defined as

$$dX/dt = F_R / N_0 \quad (16)$$

Under the steady state condition, the transport and reaction fluxes are related as

$$F_R : F_{O_2} : F_{CO} = 1 : 1.5 : 1 \quad (17)$$

After combining equations, the solution to (16) is in the same quadratic form as (6), although the coefficients A and B differ from the Deal-Grove model. As with Si, the SiC oxidation kinetics exhibit linear and parabolic growth regimes corresponding to the interface reaction or diffusion processes being the rate-controlling step. In the interface reaction limited case, the linear rate constant is approximated by

$$B/A \approx (C^g_{O_2} / N_0) k_f \quad (18)$$

In the diffusion limited case, there are two possible extremes. If oxidant in-diffusion is the rate-controlling step, then the parabolic rate constant reduces to

$$B \approx (C^g_{O_2} / 1.5 N_0) D_{O_2} \quad (19a)$$

Alternatively, if CO out-diffusion is the rate-controlling step, then the parabolic rate constant can be approximated as

$$B \approx (C^g_{O_2} k_f / N_0 k_r) D_{CO} \quad (19b)$$

It is also possible that both $O_2$ and CO diffusion processes play comparable roles in controlling the growth rate. In such a case, the parabolic rate constant is expected to obey the more general relation

$$B = N_0^{-1} (C^g_{O_2} k_f - C^g_{CO} k_r)(1.5 k_f / D_{O_2} + k_r / D_{CO})^{-1} \quad (19c)$$

The issue whether $O_2$ or CO species are responsible for the diffusion-limited growth regime is currently disputed. In fact, this is not the only unresolved matter in a general attempt to understand the intricacies of the SiC oxidation mechanism. There is disturbing variation among reported oxidation rates on SiC. Furthermore, there is overwhelming experimental evidence to suggest that atmospheric SiC oxidation is anisotropic in nature, i.e. the growth rate depends strongly on crystal orientation [4]. For instance, 4H-SiC oxidizes almost an order of magnitude slower on the (0001) Si-face compared to the (000−1) C-face in atmospheric furnaces, a phenomenon that is not predicted by current models [3,5,6]. The SiC oxidation mechanism is considerably more complicated than that of Si. Despite numerous studies, present understanding of the exact kinetics of SiC oxidation remains only educated speculation.

## 1.3. $SiO_2$/SiC structure formation and improvement efforts

Numerous studies have focused on applying conventional oxidation methods to thermally form $SiO_2$ films on SiC material. Although Si oxidation technology has been advanced and refined over the decades, there remains vast room for improvement in the growth of both SiC crystal material and oxide layers with quality interfaces before practical MOSFET power devices can be achieved on SiC. Typical $SiO_2$/SiC structures exhibit a broad range of electrical defects. Much empirical work has been performed in an attempt to reduce the amount of defects, with limited success.

### 1.3.1. Conventional thermal oxidation of SiC

Oxide films on SiC are chemically difficult to form and require growth temperatures hundreds of degrees higher than Si in standard atmospheric furnace

processes. This is due partly to the fact that Si-C bonds require higher energy to break than Si-Si bonds (290 vs. 218 kJ/mol). In fact, typical SiC thermal oxidation rates are roughly an order of magnitude slower than those of Si at the same growth temperature. Furthermore, 4H-SiC has a small lattice constant (3.08 Å) compared to that of Si (5.43 Å), a property which causes a large amount of compressive strain to develop at the interface during oxide growth. As a result, an abrupt $SiO_2$/SiC interface is not energetically favorable. Instead, the interface consists of a wide defect-filled region transitioning between the SiC lattice and stoichiometric $SiO_2$.

As mentioned previously, a principle factor that complicates the formation of $SiO_2$ films on SiC is the presence of carbon in the semiconductor material, which ideally should be removed from the system by out-diffusion of CO reaction products. However, it is generally believed that not all of the carbon products generated by the interface oxidation reaction actually out-diffuse and desorb into the gas phase, but rather some residual carbon is incorporated into the interfacial transition region or even the oxide bulk. This residual carbon is a primary suspect for the large amounts of defects and carrier traps which have thus far hindered $SiO_2$/SiC technology.

As a result of the strained lattice mismatch and residual carbon inherent in $SiO_2$/4H-SiC structures, the interfacial transition region likely contains silicon sub-oxide ($SiO_x$ , $x < 2$) and silicon oxy-carbide ($Si_xO_yC_z$) components as well as other structural and carbon-related defects, based on numerous interface studies [7-21]. The thickness of the $SiO_2$/4H-SiC transition region is believed to be on the order of 50 Å, compared to an abrupt ~5 Å oxide interface on Si. Not surprisingly, oxidation of SiC produces significantly higher interface defect densities than those achieved on Si [7,8]. To date,

the precise structure and chemical composition of the $SiO_2$/4H-SiC transitional region is unresolved.

Standard atmospheric oxidation of SiC typically involves an ambient of either dry oxygen ($O_2$), water vapor ($H_2O$) or pyrogenic steam ($O_2$ + $H_2$) at growth temperatures between 1000°C and 1300°C. Below 950°C, no thermal oxide growth is believed to occur on SiC in dry or wet oxygen ambient under standard atmospheric conditions. SiC oxidation is generally followed by a re-oxidation annealing step in dry or wet oxygen at a temperature around 950°C [7,8,22,23]. The low temperature is chosen so that no further oxidation occurs at the interface, and no additional carbon-containing reaction products are generated as a result. During re-oxidation, oxidant molecules are suspected to further react with carbon in the interface or oxide and the resulting oxy-carbide species undergo out-diffusion through the oxide, desorbing from the oxide surface to the gas phase. Re-oxidation anneals at 950°C may also allow the oxide to relax and relieve compressive stress at the interface, especially considering that the viscosity transition temperature of $SiO_2$ is around 960°C [24].

Although some improvements in interface and oxide quality have been achieved by re-oxidation, residual carbon-related defects and silicon sub-oxides still plague the defect-filled interfacial transition region. Various post-oxidation anneals [7,8,25-35] have been studied in an attempt to reduce interface trap densities ($D_{it}$). The anneals are typically performed at non-oxidizing temperatures, similar to re-oxidation annealing, and have included a variety of ambients such as nitrous oxide ($N_2O$), nitric oxide (NO), nitrogen ($N_2$), ammonia ($NH_3$), hydrogen ($H_2$), and argon (Ar), with mixed results. Anneals in NO appear to have been the most effective to date in reducing or passifying

defects in the interfacial region, yielding relatively lower $D_{it}$ values particularly near the conduction band edge in n-type 4H-SiC [25-28]. The action of atomic nitrogen is believed to be responsible for these positive, however limited, results. Compositional studies have established that the nitridation anneals (excluding $NH_3$) incorporate nitrogen in the interfacial region only, not in the oxide bulk. Despite concentrated research efforts, $SiO_2$/SiC structures formed by conventional atmospheric oxidation processes and anneals contain high levels of electrically active defects which are detrimental to device performance and have thus far stymied the great potential of SiC materials for field-effect power applications.

### 1.3.2. An alternative approach: remote plasma processing

Plasma-assisted growth of oxide films at low pressures is an appealing alternative to standard atmospheric processes. The principal advantage of such an approach is that a significant portion of the energy input required to drive a chemical process can be gained from electrons in a plasma discharge, instead of from thermal energy at the ambient process temperature. Since the production of reactive precursors, intermediates, or the final products are less dependent on thermal energy input, plasma-assisted processes can be performed at reduced temperatures which translates to production cost savings. The low pressures, reduced temperatures, and additional reactive species generated by plasma discharge imply different, and likely more complex, reaction kinetics than those in the traditional atmospheric oxidation model.

Plasma-assisted processes at temperatures as low as 400°C have been employed to grow oxide films on Si using oxygen radicals as the oxidizing species [36-38]. The reduction in growth temperature achieved is quite remarkable considering that the

thermal oxidation rate of Si is essentially zero below roughly 600°C in atmospheric furnace processes.

Oxide film growth has also been successfully demonstrated on SiC processed in flowing afterglow of a remote plasma containing oxygen species [15,39-43]. High oxidation rates at low pressures have been obtained with growth temperatures hundreds of degrees below typical atmospheric processes. As an example (table 1.2), consider a 45 minute pyrogenic steam oxidation at 1100°C which produced only 180 Å of oxide on 4H-SiC in an atmospheric furnace process [41], whereas 10 minutes of oxidative afterglow exposure at 1 Torr pressure and 850°C grew 165 Å of oxide film (figure 3.1). These results illustrated some of the advantages of a plasma-assisted oxidation approach which achieved 4× higher growth rate despite occurring at 250°C lower oxidation temperature and 3 orders of magnitude lower process pressure (proportional to growth rate per equation 13).

Table 1.2. Comparison of selected 4H-SiC thermal oxidation results from atmospheric pyrogenic steam and remote plasma processes. The afterglow oxidation process demonstrated 4× higher growth rate despited occurring at lower temperature and pressure.

| Oxidative ambient | Pressure (Torr) | Temperature (°C) | Time (min.) | Thickness (Å) | Growth rate (Å/min.) |
|---|---|---|---|---|---|
| pyrogenic steam | 760 | 1100 | 45 | 180 | 4 |
| oxygen afterglow | 1 | 850 | 10 | 165 | 16.5 |

A study of oxidative removal of organic materials [44] discovered a low 0.5 eV activation energy (EA) for atomic oxygen reacting with either polymeric or graphitic

carbon. Excited singlet molecular oxygen ($O_2$*) also exhibited an EA of 0.5 eV for reaction with polymeric carbon. Interestingly, $O_2$* reacted instantaneously at room temperature with graphitic carbon, yielding an immeasurable EA (essentially zero). An additional investigation of photo-resist stripping [45] found high etch rates of organic (i.e. containing C) polymers when exposed to a flow of oxygen microwave plasma afterglow.

The oxygen radicals and excited species produced in an oxygen plasma discharge serve a critical function in the afterglow oxidation of SiC. Namely, they participate in the oxidizing reaction at the $SiO_2$/SiC interfacial region by breaking Si-C bonds and forming Si-O bonds, which are added to the amorphous dielectric layer, and C-O products which out-diffuse through the oxide film. The proficiency of plasma-generated reactive oxygen species in attacking and removing residual carbon at or near the interfacial region is suggested to be one of the main factors contributing to the high afterglow oxidation rates achieved on SiC. The aggressive action of O radicals and excited molecules toward carbon observed in the aforementioned studies gives solid support to this theory and further illustrates why a remote plasma processing approach is particularly suited to face the challenge of growing quality $SiO_2$/SiC film structures.

In addition to using species generated by oxygen plasma discharge to grow oxide films, nitrogen radicals have also been used for treating oxides on both Si and SiC in the form of remote plasma nitridation anneals. One investigation employed a $N_2$ remote plasma treatment to nitride a thin $SiO_2$ intermediate layer prior to $HfO_2$ dielectric growth on Si, resulting in enhanced thermal stability, resistance to oxygen diffusion during rapid thermal annealing, and lower leakage [46]. In another study atomic N was used to form an ultrathin oxy-nitride dielectric film on Si with increased uniformity and reliability

[38]. A study performed on SiC found that a remote plasma nitridation anneal resulted in an improvement of interface properties of thin oxides on 4H and 6H-SiC [47]. The positive influence of atomic N in removing or passifying interfacial defects on SiC warranted an investigation of the role of N radicals in the afterglow oxidation method. This was achieved by including a nitrogen-containing source gas in the afterglow surface conditioning and oxidation media.

### 1.3.3. Surface conditioning

Knowledge and control of the SiC surface condition prior to oxidation is extremely important since the surface chemistry, morphology, structure, and electrical state have a combined impact on oxidizing reactions and formation of the $SiO_2$/SiC interface. Several surface science studies have investigated the effects of remote plasma hydrogen and nitrogen treatments on 4H and 6H-SiC surfaces at temperatures between 200°C and 750°C and pressures of 0.2–1.0 Torr [48-50]. Bare untreated SiC surfaces were found to be typically terminated with a thin (~15 Å) contamination layer containing Si-O, Si-F, C-F, and C-C bonds. Oxygen and fluorine residuals were present following a standard RCA [51] wet cleaning procedure. This was principally due to the inefficacy of hydrofluoric acid (HF) at terminating SiC surfaces with hydrogen, unlike the near-ideal hydrogen passivation of Si surfaces obtained by submersion in HF. An *in-situ* hydrogen cleaning performed by $H_2$ remote rf plasma was found to selectively interact with residual oxygen which was removed as volatile $H_2O$. Relatively clean, atomically flat and terraced SiC surfaces were achieved at lower temperatures, and surface roughness was observed to increase with hydrogenation temperature. The ability to perform plasma-assisted

hydrogen cleaning at such low temperatures (200°C−750°C) was a huge advantage compared to temperatures around 1500°C required for thermal $H_2$ etching of 4H-SiC.

SiC surfaces treated with atomic nitrogen generated by an $N_2$ remote rf plasma were modified due to incorporation of nitrogen into the SiC surface region, forming an ultrathin nitrided ($SiN_x$) overlayer. The nitridation process proceeds, similarly to oxidation, with nitrogen adsorption and surface coverage, in-diffusion through any existing nitride layer, reaction at the buried $SiN_x$/SiC interface, out-diffusion of volatile $CN_x$ products, and desorption to the gas phase. The C site is preferred for N substitution, and this N-for-C exchange results in Si-N being the stable bonding configuration at the interface. The chemisorption and reaction of nitrogen at the SiC surface induces a charge transfer between the adsorbate and semiconductor which alters the intrinsic surface charge due to structural defects and impurities. This results in a modification of the surface state density, band-bending, and electronic properties of the nitrided SiC surface, in addition to the chemical and structural alterations caused by nitride overlayer formation. The findings of these SiC surface studies motivated the application of a combination of $H_2$ and $N_2$ remote plasma treatments of SiC surfaces prior to afterglow oxidation, and an examination of the influence of remote plasma surface conditioning on subsequent $SiO_2$/SiC interface formation and film growth.

## 1.4. Capacitance-voltage characterization of oxide/semiconductor structures

Capacitance-voltage (C-V) characteristics reveal much information regarding the quality of dielectric films and interfaces on semiconductors. C-V measurements are the standard means of metrology by which to evaluate oxide electrical performance and extract various parameters of merit. Several methods of obtaining C-V characteristics are

possible, but all utilize the same basic principle. Every C-V measurement technique is capable of applying a bias voltage across the oxide/semiconductor structure and extracting the total structure capacitance as a function of potential.

### 1.4.1. Capacitance-voltage measurement fundamentals

The total capacitance ($C_{TOT}$) of an oxide/semiconductor structure is the series combination of the dielectric capacitance ($C_{OX}$) and the capacitance due to any space charge region in the semiconductor ($C_{SC}$). Interface traps can contribute a parasitic capacitance ($C_{IT}$) in parallel with $C_{SC}$. The equivalent total capacitance of the oxide/ semiconductor structure is expressed as

$$C_{TOT}^{-1} = C_{OX}^{-1} + (C_{SC} + C_{IT})^{-1} \tag{20}$$

The total applied voltage ($V_B$) used to electrically bias the structure under test is distributed between a potential drop across the dielectric insulating layer ($V_{OX}$), and a surface potential barrier associated with the semiconductor surface and space-charge region ($V_{SB}$). Figure 1.3 portrays a schematic representation of this simple electrical model for an oxide/semiconductor structure.

For the purpose of illustration, consider $C_{TOT}$ of an oxide film grown on negatively-doped semiconductor material, with electrons serving as majority carriers. With a large positive applied bias ($V_B >> 0$), a positive electric field develops across the oxide ($V_{OX} > 0$), and electrons are accumulated at the semiconductor surface inducing a positive surface barrier ($V_{SB} > 0$). As a result, electron energy bands are bent downward in the semiconductor near the interface (figure 1.4a). Assuming an ideal structure without interface traps, the measured capacitance in accumulation ($C_{ACC}$) will be that of the oxide

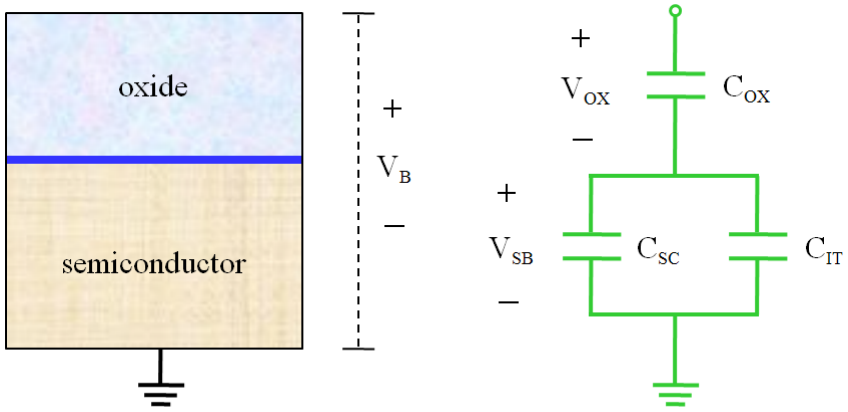


Figure 1.3. Electrical model for the capacitances and potentials associated with an oxide/semiconductor structure.

layer alone since no space-charge region exists in the semiconductor. With the measured capacitance normalized per unit area,

$$C_{ACC} = C_{OX} = \varepsilon_0 \varepsilon_r / t_{OX} \tag{21}$$

where $\varepsilon_0$ is the permittivity of vacuum, $\varepsilon_r$ is the relative permittivity of the dielectric, and $t_{OX}$ is the oxide film thickness. For a large negative applied bias ($V_B << 0$), a negative electric field develops across the dielectric ($V_{OX} < 0$), and electrons are repelled from the interface into the semiconductor, which becomes depleted of majority carriers in the surface region. The resulting negative surface barrier ($V_{SB} < 0$) corresponds to electron energy bands bending upward in the semiconductor near the interface (figure 1.4b). At the transition between accumulation and depletion of majority carriers near the semiconductor surface is a state termed "flat-band" because no bending occurs in the electron energy bands (figure 1.4c). Under ideal assumptions (i.e. without any contribution from charged defects), the applied bias at the flat-band condition ($V_{FB}$) is equal to a relatively small workfunction difference ($\Phi_{MS}$) between the semiconductor and the probe or gate metal used in the particular C-V measurement.

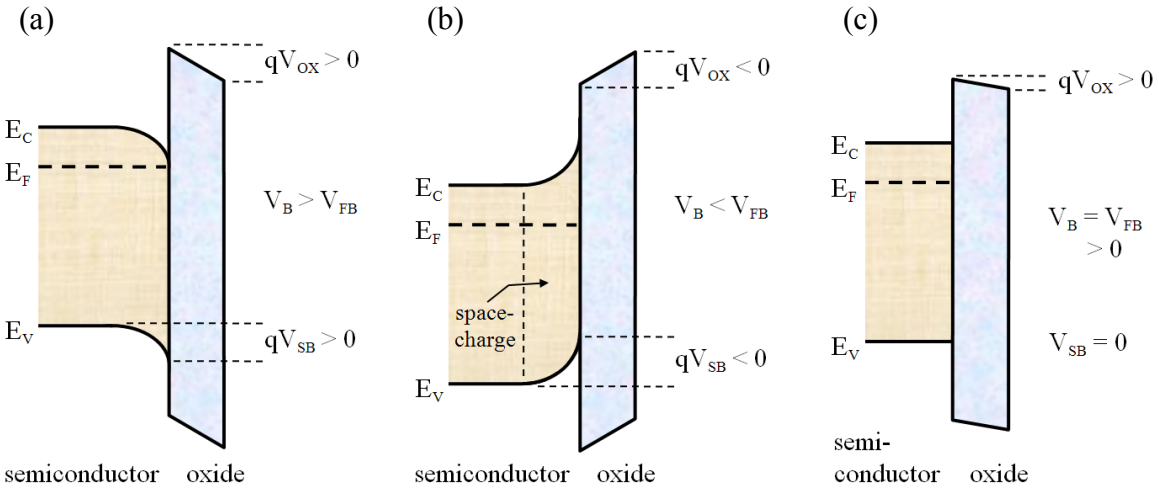


Figure 1.4. Electron energy band diagrams representing accumulation (a), depletion (b), and flat-band condition (c) of an oxide/semiconductor structure under applied bias.

$$V_{FB} = \Phi_{MS} \quad \text{(ideal)} \tag{22}$$

Under the depletion condition, a space charge region exists in the semiconductor whose added capacitance $C_{SC}$ in series with $C_{OX}$ results in a lower measured $C_{TOT}$. As $V_B$ becomes increasingly negative, the semiconductor depletion region widens and the energy bands are bent further upward. The decreasing $C_{SC}$ associated with a widening space-charge region causes $C_{TOT}$ to continually decrease toward lower capacitance values as the the semiconductor is further depleted ($C_{DEP}$). A typical C-V response of an oxide on n-type semiconductor material is depicted in figure 1.5, illustrating the parameters $V_{FB}$, $C_{FB}$, $C_{ACC}$, and $C_{DEP}$. When considering a non-idealized oxide structure with electrically active defects present, the general effects on a C-V measurement are basically twofold. First, any interface traps will cause a stretch-out of the C-V curve around the flat-band as the structure is swept between the extremes of accumulation and depletion conditions. This stretch-out occurs because some charge is trapped in the process of filling or emptying interface states distributed at various energy levels throughout the

band-gap, rather than further accumulating or depleting the semiconductor (depending on sweep direction). Second, any oxide trapped charge or fixed charge will induce a horizontal translation of the C-V curve along the voltage axis, effectively shifting $V_{FB}$ from its theoretical value. A certain amount of applied bias is required to supply the charge needed to compensate for the charged oxide defects and achieve flat-band condition. The flat-band voltage shift ($\Delta V_{FB}$) due to net oxide charge ($Q_{TOT}$) is related to $C_{OX}$ :

$$V_{FB} = \Phi_{MS} + \Delta V_{FB} = \Phi_{MS} + Q_{TOT} / C_{OX} \tag{23}$$

The effects of $D_{IT}$ stretch-out and a flat-band shift due to negative $Q_{TOT}$ on n-type C-V curves are illustrated in figure 1.5.

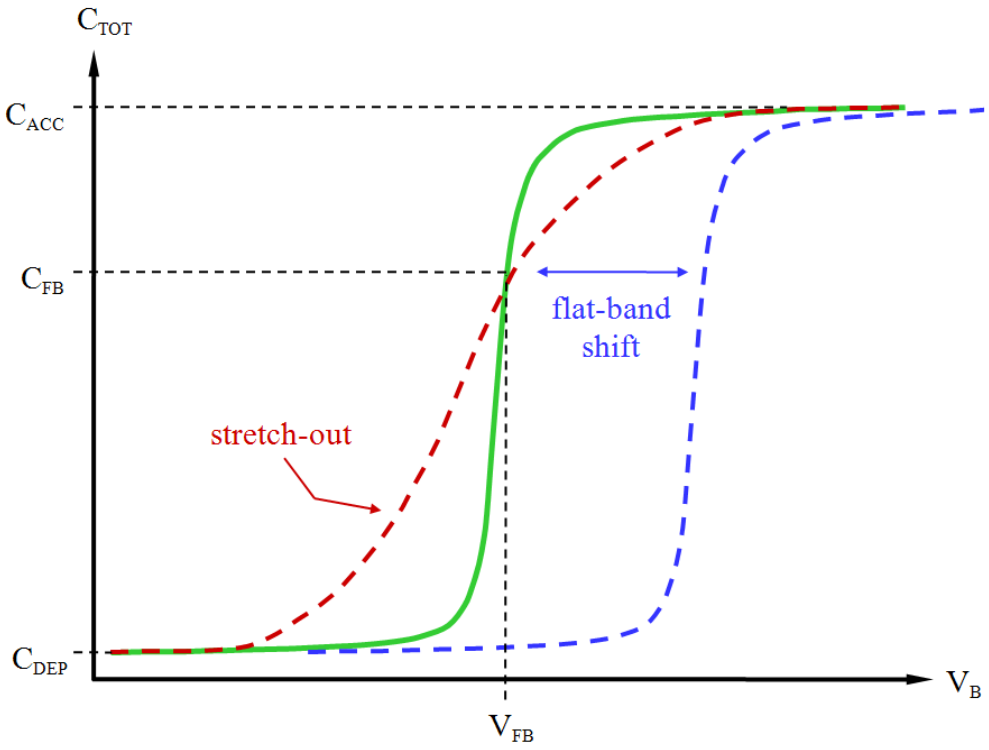


Figure 1.5. Oxide C-V characteristic example on n-type semiconductor, illustrating the effects of C-V stretch-out and flat-band shifting.

The saturated value of capacitance measured with the semiconductor surface strongly accumulated is typically used to extract the electrical equivalent oxide thickness (EOT) of a dielectric film. EOT is the equivalent thickness of $SiO_2$ which would yield a measured $C_{ACC}$. Although permittivities of amorphous $SiO_2$ can fall in the range $\varepsilon_r = 3.7 - 5.1$, a general value of $\varepsilon_r = 3.9$ is assumed for stoichiometric $SiO_2$. Hence, EOT is extracted from $C_{ACC}$ by re-arranging (21) as follows:

$$EOT = 3.9\varepsilon_0 / C_{ACC} \tag{24}$$

### 1.4.2. Contact vs. non-contact metrology

Any method for measuring C-V oxide characteristics requires a means to apply a biasing potential across the oxide/semiconductor structure. This is conventionally achieved by the deposition of metal (e.g. Al) or poly-crystalline silicon (poly-Si) conducting films on the oxide surface in order to fabricate gate contacts for MOS capacitor test structures (figure 1.6a) or MOSFET devices. A voltage applied through an electrical probe contacting the gate serves to bias the oxide/semiconductor structure when the substrate is grounded. Determination of capacitance is possible using appropriate measurements of voltage, current, and/or impedance parameters.

The requirement of device fabrication for contact C-V measurements means that these techniques are invasive, destructive, and limit the possibility of continued processing following determination of oxide quality. Test wafers are usually recycled or discarded following oxide metrology, which adds an enormous burden of production cost and time. The additional process time is particularly cumbersome in the research and development stage, when quick feedback is crucial to the optimization of novel material processes.

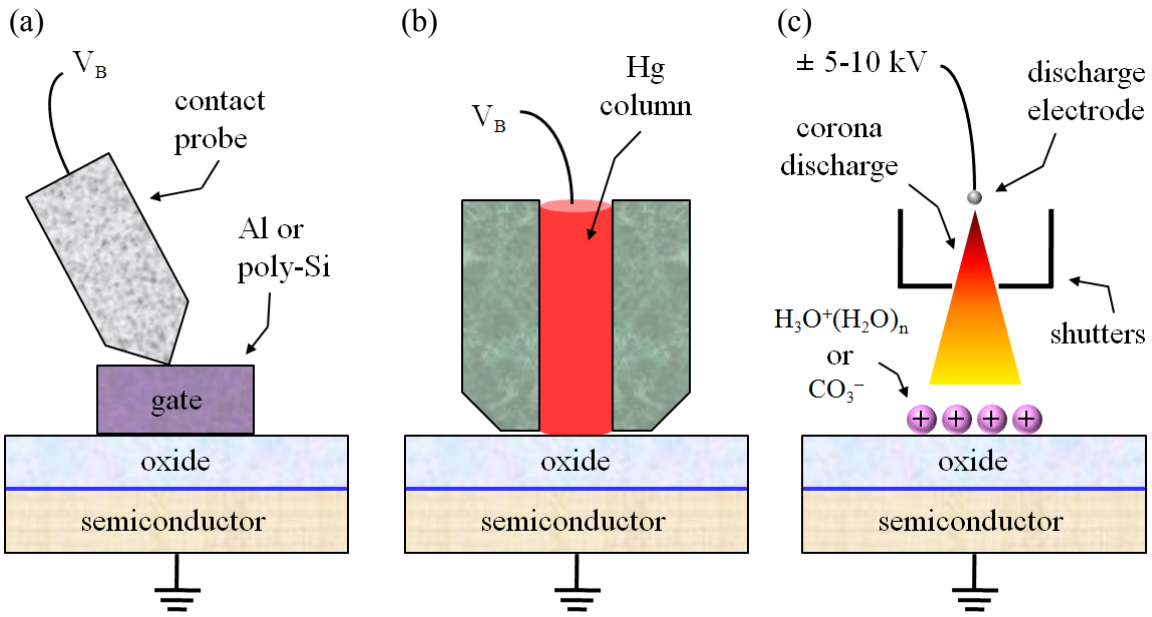


Figure 1.6. Alternative techniques of generating a bias potential across an oxide/ semiconductor structure: MOS contact (a), Hg-probe (b), and corona ion deposition (c).

A liquid mercury (Hg) probe is capable of providing a temporary electrical contact to an oxide surface (figure 1.6b). Thus, Hg-probe C-V measurements allow oxide characterization without test structure fabrication. However, the Hg-probe technique leaves residual Hg metal contamination on the oxide surface following measurement. Due to the problem of mercury contamination, Hg-probe measurements should be classified as destructive in nature. Subsequent fabrication steps cannot be performed without jeopardizing oxide and process cleanliness.

An in-line metrology technique based on the deposition of corona ions on a surface and monitoring of the structure potential with a non-contacting probe provides many advantages over contact measurement methods. The corona-Kelvin metrology (C-KM) approach [42,43,52-59] is fast, non-destructive, and can be applied to obtain oxide electrical characteristics at selected points in a sequence of processes. The C-KM

technique is based on the use of charged ions ($CO_3^-$ or $H_3O^+(H_2O)_n$ ) generated by corona discharge in air, and deposited on a sample surface (figure 1.6c). The corona ions energy is reduced by ambient collisions such that they are non-damaging when arriving at the sample surface [60], and can be completely removed without residual contamination by rinsing in de-ionized (DI) water. The deposited corona surface charge accomplishes electrical biasing of an oxide/semiconductor structure, analogous to the gate contact of MOS C-V measurements. Monitoring of the deposited charge, combined with potential determination by a non-contacting voltage probe, produces charge and voltage information useful for extracting many semiconductor and oxide parameters of merit, including the capacitance response. Thus, the C-KM method is a truly non-invasive and non-damaging technique capable of in-line electrical monitoring of dielectrics and semiconductors, and a valuable tool for obtaining quick C-V characteristics of oxide films on semiconductors.

The focus of this work is the growth and characterization of oxide thin films on 4H-SiC using the unique capabilities of remote plasma afterglow processing technology and in-line C-KM, with emphasis on the role of semiconductor surface conditioning prior to oxidation. A general attempt has been made to apply the oxidation mechanism knowledge and process technology that have been developed successfully for the $SiO_2$/Si system to the oxidation of the WBG compound semiconductor SiC, with less than satisfactory results. Although SiC is an attractive candidate for power and other applications, most importantly the 4H polytype, numerous defects exist in $SiO_2$/4H-SiC structures, and the precise interfacial chemistry, structure, and origin of defects is not presently understood. Remote plasma afterglow processing at low pressure and reduced

temperatures offers an advantageous, flexible and effective alternative to conventional atmospheric furnace processes for growing oxide films on SiC. High growth rates at reduced temperatures are achievable, and the possibility exists for sequential *in-situ* processing steps, including surface treatment prior to oxidation which could have a significant impact on the $SiO_2$/SiC interface formation and oxide growth process. A non-contact corona-Kelvin metrology technique may be used as a quick, non-destructive means for performing electrical characterization of semiconductors and experimentally grown oxide films, and to evaluate structure quality at various points in a process sequence due to its non-invasive nature.

# Chapter 2. Experimental Approach

The experimental methods used in this work included 4H-SiC surface conditioning and growth of dielectric films and utilized a remote plasma-assisted sequential processing approach in an afterglow chemical reactor. The resulting oxide/SiC structures were characterized using non-contact corona-Kelvin metrology capacitance data to evaluate key oxide parameters such as film thickness, flat-band voltage, uniformity, and trapped charge. In addition, C-KM depletion voltage transients and X-ray photoelectron spectroscopy (XPS) analysis of the conditioning stage preceding oxidation yielded electrical and chemical information regarding the effects of remote-plasma treatment on the SiC surface. The compiled results were used to investigate the effects of strategically selected process variations, and gain a better understanding of the afterglow surface treatment and oxidation of SiC.

## 2.1. Afterglow chemical processing

As introduced previously, the use of an afterglow chemical reactor for remote plasma processing offered an advantageous alternative to a conventional atmospheric oxidation furnace, and facilitated oxide film growth at temperatures hundreds of degrees lower than possible with thermal energy input alone. The added flexibility of sequential *in-situ* processing capability combined with a wide variety of possible chemical ambients provided important tools for controlling and manipulating the initial surface condition, interface formation, film growth and post-oxidation environment.

2.1.1. Afterglow apparatus description and operation

The afterglow chemical reactor [61] used in this work operated as a 1 Torr vacuum furnace system with a flowing reactive ambient including excited and atomic gas species generated by microwave plasma discharge upstream from the heated substrates. A schematic representation of the afterglow apparatus is shown in figure 2.1.

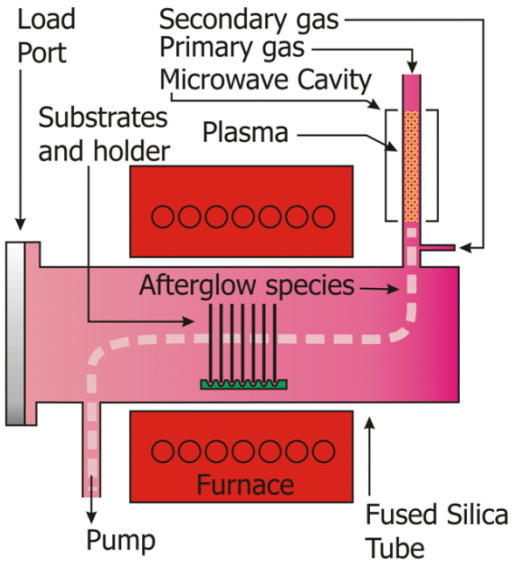


Figure 2.1. Schematic diagram of the remote plasma afterglow apparatus.

A resistive heating furnace surrounds a 6-in. diameter fused silica tube and maintained the substrates at a desired temperature, up to 1200°C. The temperature inside the furnace zone was monitored at multiple points simultaneously using thermocouples spaced along a profile rod. Substrate 4H-SiC wafers (typically 3-in. diameter) were positioned vertically by slots in a quartz loading boat contained in the growth zone. The substrate or wafer area was perpendicular to gas flow, with the (0001) Si-face directed downstream by convention. A protocol of surrounding the SiC substrates with additional

Si shielding wafers on either side was enforced to reduce turbulence and increase uniformity of film growth.

A rotary-vane mechanical pump backing a series roots blower evacuated the growth chamber to 1 Torr total pressure with a combined flow of source gases approximately 4 standard liter atmospheres per minute (slam). This enabled a high mass flux of reactants in the wafer region and a short transit time of neutral species from generation in the microwave plasma to the furnace zone. Precise mixtures of desired source gases were generated using an array of mass flow controllers. The system pressure was monitored both by a capacitance monometer and thermocouple on the exhaust side of the furnace zone, and controlled by adjusting an exhaust valve which altered the rate of pumping.

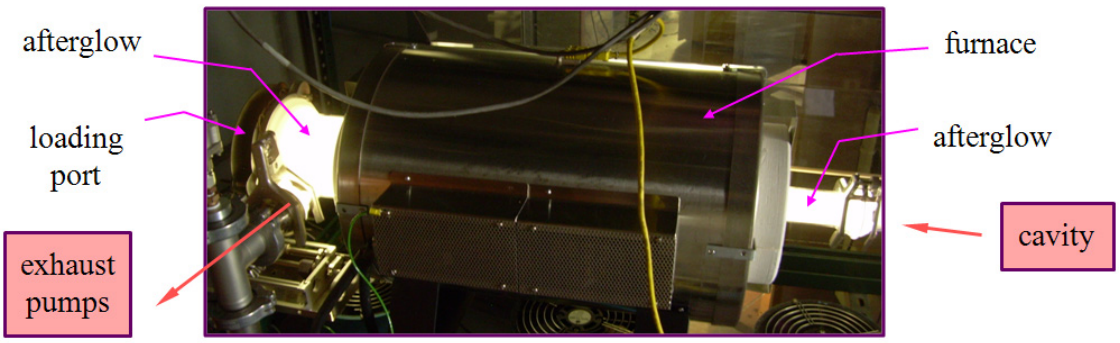


Figure 2.2. Photographic image of the remote plasma apparatus furnace zone during operation, with visible chemo-luminescence of afterglow excited species.

Figure 2.2 contains a photographic image of the furnace portion of the afterglow apparatus during operation. The visible chemo-luminescence eminating from the fused-silica enclosure may be observed entering and exiting the furnace growth zone. This luminescence was caused by photon emission processes associated with electrons in excited states returning to lower energy orbitals. As witnessed in the image, the lifetimes

of excited afterglow species were much longer than required to transport downstream from the plasma discharge and react with substrates in the furnace zone.

The core of the afterglow reactor was a multi-mode excitation cavity surrounding a quartz tube containing flowing source gases upstream from the furnace zone. A remote continuous-wave 2.45 GHz microwave source acted to drive the excitation cavity through a series of waveguide sections and an injecting rod inserted an adjustable distance into the cavity interior. The microwave excitation established inside the cavity generated a plasma discharge in the flowing gaseous species. A forward power around 1 kW was typically required to maintain a stable plasma state. The forward and reverse power and coupling between the microwave source and cavity were tuneable by varying the high-voltage supply power, waveguide tuning stubs, and cavity injection rod distance.

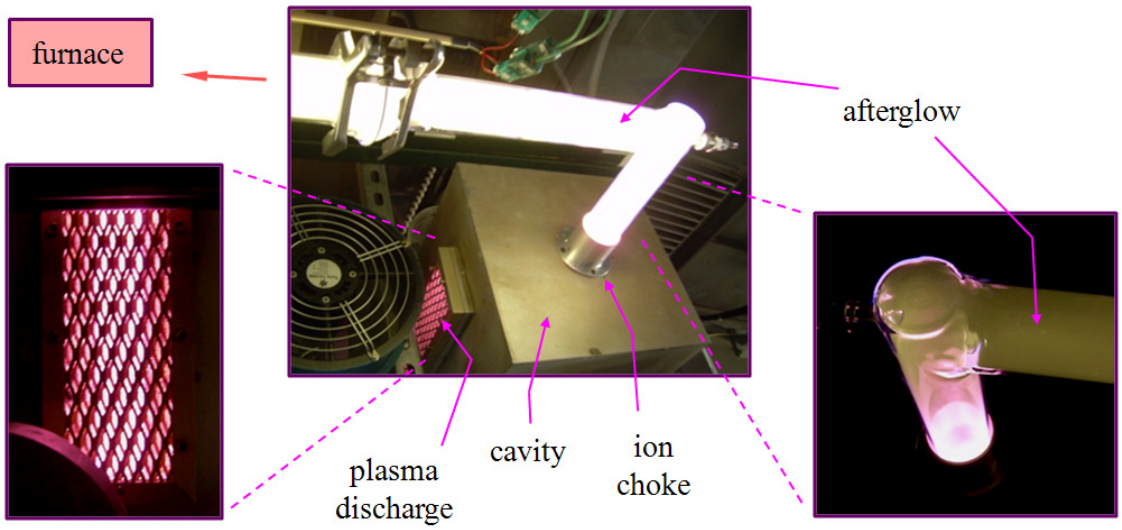


Figure 2.3. Photographic images of the remote plasma apparatus microwave cavity, depicting the plasma discharge and afterglow during operation.

The microwave plasma discharge created a rich collection of excited molecular and atomic gaseous species, ions, electrons and photons. Charged species (i.e. ions and

electrons) were contained inside the excitation cavity using an RF choke formed by a grounded metallic ring at the cavity exit. A right-angle bend in the quartz tubing between the cavity and furnace prevented photon radiation, particularly damaging ultra-violet (UV) frequencies, from entering the growth zone. Some residual amount of UV radiation, however, did travel down the walls of the quartz tubing toward the growth zone and was blocked by a fitting that joins the quartz plasma tube and furnace tube. Thus, the only plasma-generated species which were permitted to reach the growth zone were neutral molecules and radicals, some being in excited electronic states. Photographic images of the microwave cavity, plasma discharge, and afterglow are shown in figure 2.3.

### 2.1.2. Dielectric growth by remote plasma sequential processing

The ability to apply alternate chemistries and temperatures in sequential *in-situ* processing steps make the afterglow method a powerful tool for growth and improvement of oxide/4H-SiC structures. The afterglow chemical reactor has the capability to provide pre-oxidation surface conditioning, oxidative growth, and post-oxidation annealing environments in a continuous process. This flexibility does not exist in conventional thermal oxidation methods using standard chemistry.

Typical afterglow oxidation processes used in this work (figure 2.4) consisted of the following general sequence schedule example:

1) load wafers under $N_2$ flow at temperature $T_{load}$ (600°C),
2) surface conditioning step at relatively low temperature $T_{cond}$ (600°C),
3) oxidation step at a higher temperature $T_{oxid}$ (850°C),
4) inert annealing step at temperature $T_{anneal}$ (1000°C),
5) unload wafers under $N_2$ flow at a temperature $T_{unload}$ (600°C).

Furnace temperature ramps were usually performed with an inert ambient flow (e.g. Ar). Please note that steps 2-4 are optional, and the temperature, duration, and chemistry of each step may be varied as desired.

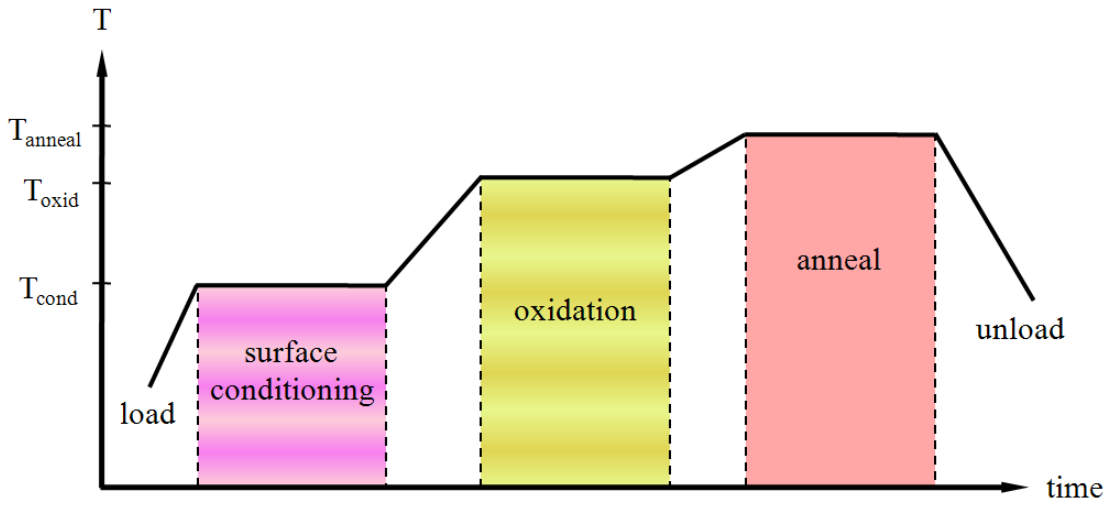


Figure 2.4. Example of a general afterglow process flow temperature profile, including pre-oxidation surface treatment, oxide growth, and post-oxidation annealing steps.

Prior to loading in the afterglow furnace, wafers were subjected to a rigorous wet cleaning procedure including piranha (2:1 $H_2SO_4$:$H_2O_2$) and dilute HCl rough cleaning, followed by a standard RCA [51] fine cleaning process using basic and acidic solutions of hydrogen peroxide to remove particles, organics, and metals from the semiconductor surface. The wet cleaning protocol ended with submersion in dilute HF to ensure removal of any oxide layer formed during chemical cleaning. However, this step was known to leave residual flurine and oxygen contaminants on the SiC surface [50], a fact to consider during subsequent afterglow processing.

The primary surface treatment used in this work was chemistry from a plasma discharge of 5% $H_2$ in balance $N_2$, a source gas mixture labeled with the common name

"forming gas" (FG). Other conditioning treatments included the afterglow ambient from pure $N_2$ remote plasma, as well as a non-excited $N_2$:$O_2$ 7:1 gas mixture. Treatment temperatures of 400°C−800°C and durations of 2.5−20 min. were investigated as variations of the standard treatment which occurred at 600°C for 20 min.

The surface conditioning step attempted to take advantage of the cleaning and nitriding effects of radicals and excited species. Reactive hydrogen along with $N_2$* and N radicals were suspected to be available for reaction with the SiC surface. The roles of hydrogen and nitrogen in a remote plasma treatment could be crucial to controlling the SiC surface in preparation for subsequent oxidizing processes.

Oxidative chemistries consisted of a remote plasma discharge of $O_2$, mixed with other additive gases. Previous studies have shown that the addition of a small percentage of nitrous oxide ($N_2O$) to an oxygen discharge resulted in an increase in atomic oxygen production and plasma stability [36]. Hence, the use of an excited ($O_2$:$N_2O$)* 4:0.3 oxidation media induced a significant increase in growth rate compared to remote plasma processes with pure $O_2$ discharge [40]. An additional growth rate increase was observed when adding FG to the ($O_2$:$N_2O$)* plasma. The standard oxidation chemistry used in this work was ($O_2$:$N_2O$:FG)* 3:0.23:0.5. Oxidation temperatures of 600°C−850°C and durations of 10−90 min. were investigated.

This work also examined the impact of post-oxidation anneals on resulting oxide quality, as a function of surface condition prior to oxidation. A typical annealing step utilized non-excited Ar gas, absent any energy from a remote plasma discharge, at a high temperature such as 1000°C for 60 min. duration. High-temperature anneals in inert Ar ambient were used to analyze the stability of afterglow-formed oxides to high-

temperature stresses which are required for subsequent fabrication steps (e.g. thermal annealing of deposited poly-Si gate film or silicide formation).

Following every oxidation process, the wafers were unloaded from the reactor under $N_2$ flow, and allowed to cool. An HF vapor etch was typically used to remove oxide from the wafer backside (i.e. C-face) to ensure electrical contact between the substrate and measurement chuck. The wafers were rinsed in DI water and dried under $N_2$ flow following backside etching. This procedure left the frontside oxide surface in an assumedly repeatable and constant condition following every growth experiment. This was an important factor related to subsequent non-contact C-KM metrology, which relies on precise control of surface charge.

## 2.2. Non-contact corona-Kelvin metrology

Electrical characterization of processes and oxide/SiC structures fabricated in this work included capacitance and voltage transient measurements performed by the non-contact corona-Kelvin method. The C-KM technique provided quick, non-invasive, electrical feedback by combining corona ion deposition and non-contact potential monitoring. This important in-line metrology technique, now common in the Si integrated circuit industry, has been adopted to facilitate measurement of SiC materials.

### 2.2.1. Corona-Kelvin tool operation and basis of measurement

The modified Semiconductor Diagnostics, Inc. Film Analysis and Substrate Testing (FAaST) 230 [62] tool used in this work was capable of performing a variety of semiconductor and dielectric measurements. As previously introduced, the tool achieved electrical biasing of the measured structures by depositing non-damaging ions in the form

of carbonate or hydrated hydronium ($CO_3^-$ or $H_3O^+(H_2O)_n$ ) on the sample surface from a high-voltage (± 5-10 kV) corona discharge in air. The structure potential was monitored in a non-contact fashion by a contact potential difference (CPD) probe.

The non-contact voltage probe applied the Kelvin method [63] of acquiring the CPD between a reference electrode and the grounded sample substrate ($V_{CPD}$). Using a Monroe configuration [64], mechanically vibrating shutters acted to periodically vary the capacitance between the electrode and substrate ($C_0$). The variable capacitance induced an alternating current ($J_{ac}$) in the electrode which was proportional to $V_{CPD}$ and is expressed as

$$J_{ac} = (V_{DC} + V_{CPD})\, C_0 \sin(\omega t) \tag{25}$$

where ω is the frequency of shutter vibration, and $V_{DC}$ is an external bias voltage applied to the reference electrode. Measurement electronics adjusted $V_{DC}$ to achieve the null current condition ($J_{ac} = 0$) in which case the sum term on the rhs of equation (25) was zero, and hence the applied bias was equal to $-V_{CPD}$:

$$V_{CPD} = -V_{DC} \tag{26}$$

Non-contact measurement of an oxide/semiconductor structure yielded a $V_{CPD}$ approximated as:

$$V_{CPD} = \Phi_{MS} + V_{OX} + V_{SB} \tag{27}$$

where, as previously, $\Phi_{MS}$ is the workfunction difference between the electrode and substrate, $V_{OX}$ is the oxide voltage, and $V_{SB}$ is the surface potential barrier. Note that in the absence of an oxide film, the measured $V_{CPD}$ should equal the surface barrier $V_{SB}$, offset by the small constant $\Phi_{MS}$ (< 1V). A schematic illustration of the CPD probe apparatus is shown in figure 2.5.

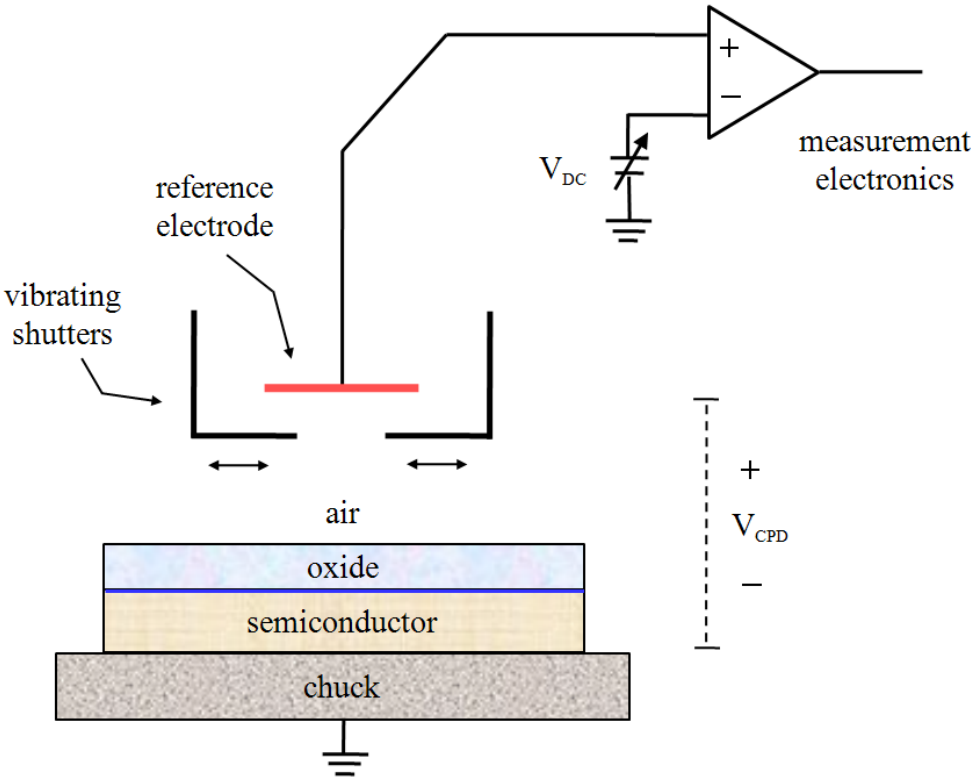


Figure 2.5. Non-contact CPD probe schematic.

In the FAaST tool, the test sample was held by vacuum on a motorized chuck, enabling multiple point measurement and wafer mapping. The ion source and CPD probe were positioned on a shuttle mechanism which facilitated the charge and measurement cycle. After the corona source deposited a precise and monitored dose of corona charge ($\Delta Q_C$), the adjacent CPD probe shifted over the same surface site to allow immediate $V_{CPD}$ measurement. The first $V_{CPD}$ reading occurred less than 1 sec. after the corona charge deposition, and the $V_{CPD}$ transient was monitored for a specified time interval following the initial reading. The $V_{CPD}$ voltage transient gave useful information regarding carrier transport and charge compensation processes when acquired over a significant time interval following a large corona charge dose pulsing the semiconductor into strong

depletion. This is the topic of discussion in chapter 4 where the electrical state of the SiC surface following conditioning treatments was examined using depletion $V_{CPD}$ transient decays.

For the purposes of oxide film characterization, capacitance data were obtained using an alternating sequence of incremental corona applications and $V_{CPD}$ determination. After each corona charge dose ($\Delta Q_C$) was deposited, the $V_{CPD}$ was monitored for 2.5 sec. Repetition of the charge and measure cycle resulted in a set of voltage transients such as those depicted in figure 2.6 obtained on an oxidized p-type SiC epi-layer. In the example measurement, the structure initially had a net negative corona charge density ($Q_C < 0$) on the surface, and was swept from accumulation to depletion condition as repeated doses of positive corona charge were deposited on the oxide surface.

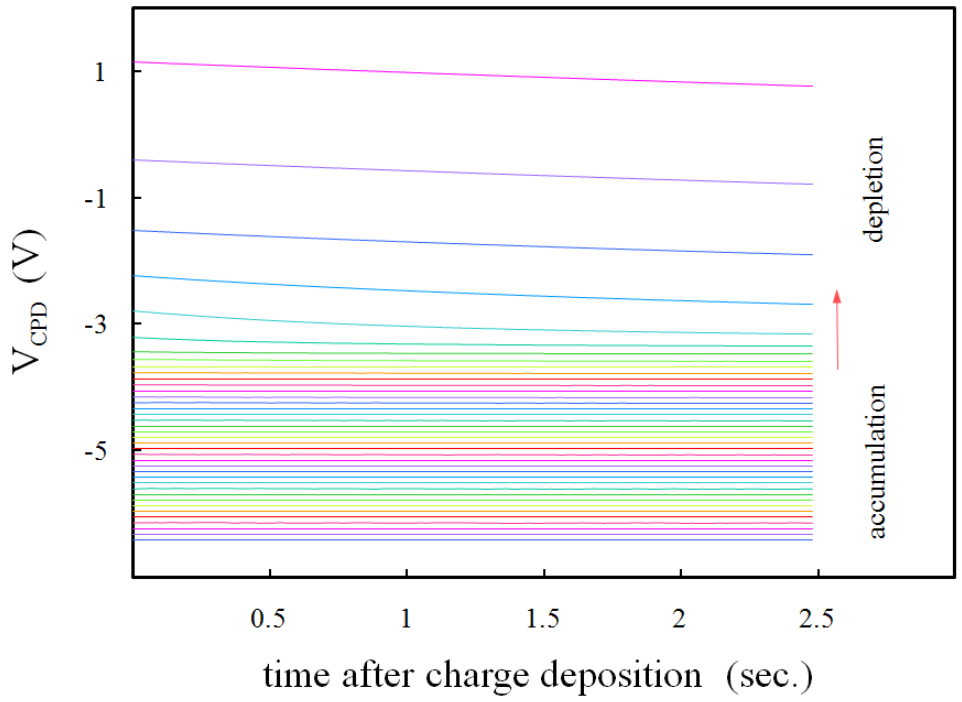


Figure 2.6. Typical $V_{CPD}$ data obtained during corona-Kelvin metrology of an oxidized p-type SiC epi-layer. Repeated doses of positive corona charge were used to sweep the structure from accumulation to depletion.

When combined with the precise monitoring of corona charge doses, the voltage data were used to generate the V-Q dependence such as that shown in figure 2.7, where the structure $V_{CPD}$ is given as a function of total surface corona charge density $Q_C$. Each data point corresponds to a single positive corona charge dose as the oxide/p-SiC structure was swept from accumulation to depletion. The V-Q relationship lies at the foundation of the corona-Kelvin metrology technique.

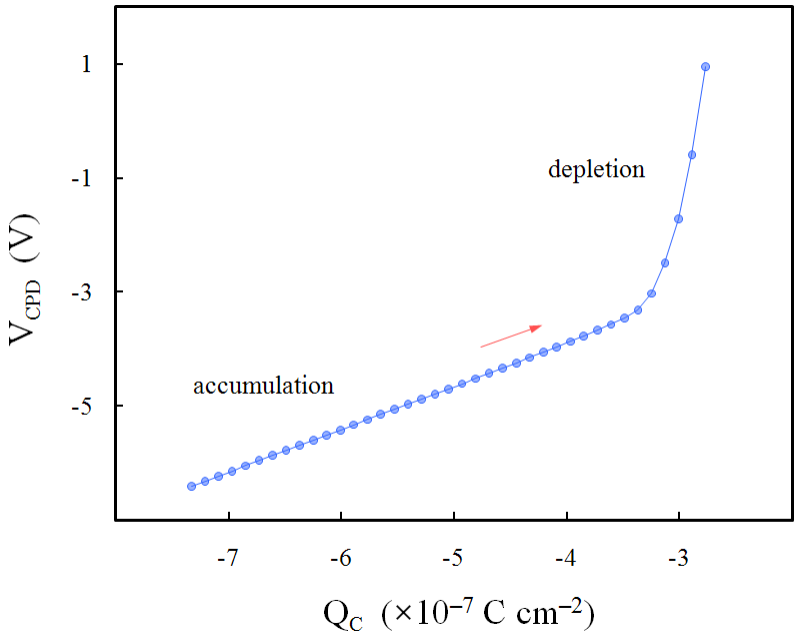


Figure 2.7. Typical V-Q response obtained during corona-Kelvin metrology of an oxidized p-type SiC epi-layer. Repeated doses of positive corona charge were used to sweep the structure from accumulation to depletion.

The structure capacitance (C) was extracted from the relationship between the $Q_C$ increment and the change in $V_{CPD}$:

$$C = \Delta Q_C / \Delta V_{CPD} \tag{28}$$

which is simply the inverse slope of the V-Q curve. A plot of C vs. $V_{CPD}$ such as that in figure 2.8 revealed the capacitance behavior of the oxide/semiconductor structure over a

voltage range depending on the polarity of deposited $Q_C$ and number of charge doses. The C-V response, as extracted from the V-t and V-Q data, was used for electrical evaluation of oxide film parameters.

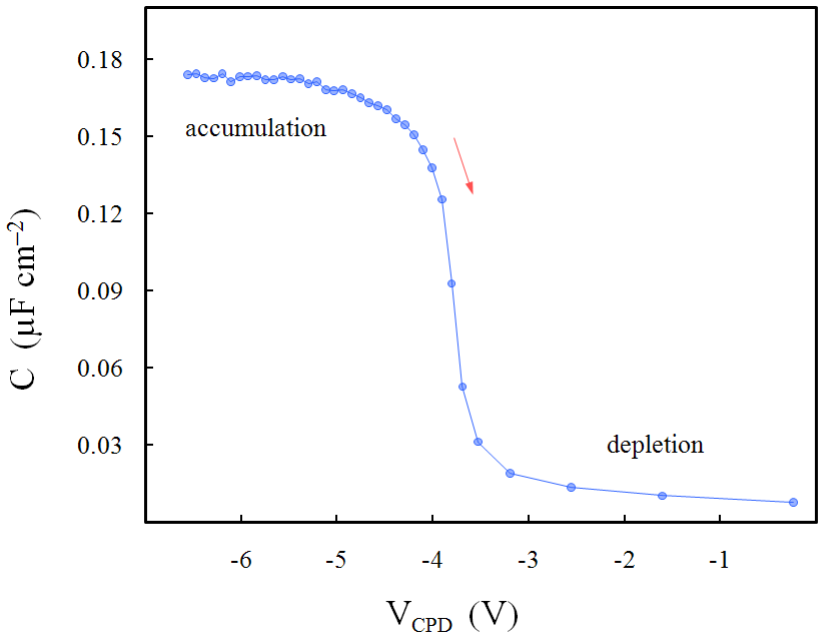


Figure 2.8. Typical C-V characteristic extracted from corona-Kelvin metrology V-Q data on an oxidized p-type SiC epi-layer. Repeated doses of positive corona charge were used to sweep the structure from accumulation to depletion.

The corona-Kelvin tool, as it was configured for SiC measurements, possessed the capability to perform non-contact C-V measurements with the sample either in ambient darkness or under strong illumination provided by a UV ($\lambda$ = 370 nm) diode. The value of $C_{ACC}$ measured on an illuminated oxide/SiC sample was used to extract the electrical film thickness. The UV diode generated photons with energy of 3.4 eV, just larger than the 4H-SiC band-gap (3.26 eV). The oxide was transparent to the photons, which were absorbed in the SiC and generated electron-hole pairs, thus eliminating any residual space-charge in the semiconductor. This ensured the oxide film was the sole contributor

to the measured structure capacitance, with the oxide potential remaining unaffected by the illumination process.

### 2.2.2. Oxide/4H-SiC structures: typical non-contact capacitance-voltage behavior

Figure 2.9 contains typical non-contact C-V results demonstrating the electrical behavior of afterglow oxide thin films on 4H-SiC. The curves shown were measured sequentially at a single site on an oxidized p-type epi-layer. Prior to any corona charge application, the structure was in a slightly depleted condition, with a small initial $V_{CPD}$ less than a volt in magnitude, implying a small amount of positive oxide charge. The polarity of $Q_C$ for the first sweep was chosen to drive the structure toward accumulation, negative for the example p-type semiconductor. The initial sweep into accumulation was a shallow sloped ramp, as many surface states and near-interface traps were charged. Following the initial sweep, the SiC was slightly accumulated, and a second sweep of opposite polarity was performed to bring the structure into depletion (positive for p-type). The process of alternating negative and positive sweeps was repeated several times to obtain a series of C-V curves, each one stressing the structure deeper into accumulation. The subsequent sweeps directed toward accumulation did not display the dramatic stretch-out that was visible during the initial sweep, indicating a satiation of the majority of interface traps. Also, the $V_{FB}$ of each sweep toward depletion was generally larger in magnitude than the sweep toward accumulation that preceded it. Furthermore, as the structure was stressed deeper and deeper into accumulation at each subsequent C-V measurement, the $V_{FB}$ increased in magnitude. The $V_{FB}$ saturated at a maximum magnitude when the structure was stressed to very strong accumulation.

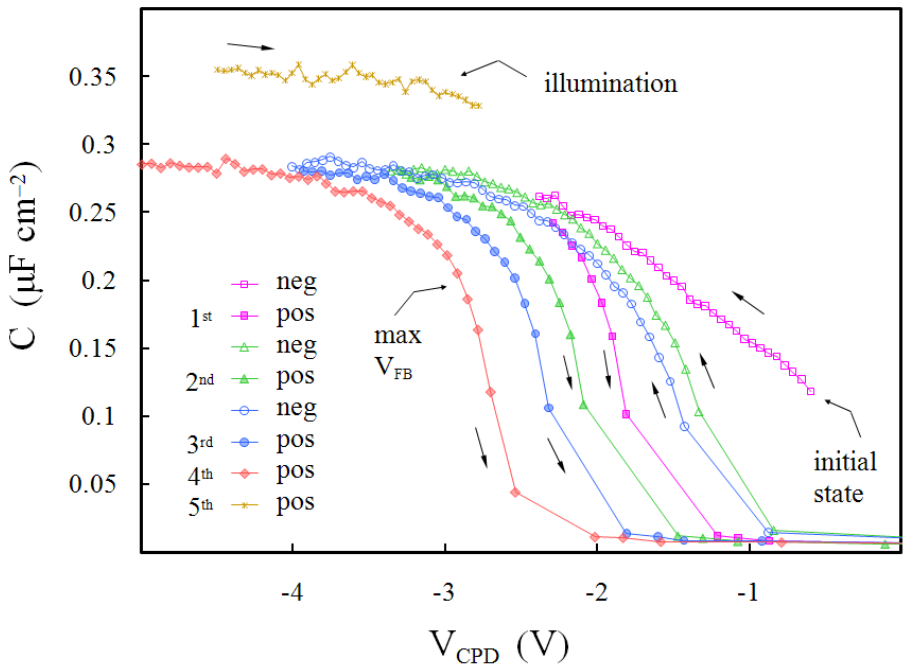


Figure 2.9. Typical non-contact C-V curves obtained sequentially at a single measurement site on oxidized p-type 4H-SiC. The measurement order of positive and negative sweeps is indicated in the legend. All except the last sweep (illuminated) were measured in darkness.

This behavior of permanent $V_{FB}$ shifting due to accumulation stress was believed to be caused by charging of transitional or near-interface traps, also called border traps. These border traps were probably related to the wide, defect-filled transition region at the interface, but they did not behave as typical interface traps which should fill and empty during each alternating sweep into accumulation and depletion, causing stretch-out of the C-V curve. On the contrary, these border traps, once filled with majority carriers during accumulation, retained their charge even when the semiconductor returned to depletion, causing a permanent $V_{FB}$ shift toward accumulation (i.e. larger magnitude $V_{FB}$). It was possible to recover the majority of border traps to their unfilled states by sweeping into depletion with the structure under strong UV illumination. In other words, after a C-V

measurement in light, the structure behaved similarly to its initial condition prior to any corona charging.

The measured $C_{ACC}$ value with the structure under strong illumination was used to extract the electrical thickness value. This was more crucial on p-type than on n-type samples, because both the p-type and n-type 4H-SiC material used in this work were epitaxial films grown on heavily doped n-type bulk substrates. Considering the p-type epitaxial layer, a parasitic series capacitance existed due to space charge at the buried $p^-/n^+$ epi/bulk junction, which effectively lowered the measured total structure capacitance. Under illumination, the buried space charge region was eliminated and the measured capacitance rose to its expected value of $C_{OX}$, as witnessed in the figure. In addition to detailed electrical measurements at single points, simple multiple-point C-V scans were performed both in dark and illuminated ambient conditions in order to investigate the uniformity of EOT and $V_{FB}$ parameters across the wafer.

This work used various figures of merit, obtained primarily by non-contact corona-Kelvin metrology, to analyze the effects of specific process variations in remote plasma surface conditioning and oxidation of SiC material. The role of nitrogen and hydrogen in pre-oxidation surface treatments were emphasized, with the aid of $V_{CPD}$ depletion voltage transient data and XPS analysis of conditioned surfaces. The effect of annealing as a test of stability to high temperature stresses was also considered. Metrology parameters including EOT, $V_{FB}$, flat-band shifting, uniformity, temperature stability, surface barrier decay, and surface chemistry were used as tools for elucidating the mechanisms involved in the plasma-assisted surface conditioning, oxide interface formation, and film growth on 4H-SiC.

# Chapter 3. Corona-Kelvin Capacitance Metrology of Afterglow Oxide Films

A variety of experiments have been performed to investigate oxide/4H-SiC structures formed by the afterglow method. Non-contact C-V characteristics obtained by corona-Kelvin metrology were used to measure the impact of process variations on growth rate, charge trapping, uniformity, and stability to temperature stress. Experiments were designed to focus on the role of nitrogen and hydrogen in the remote plasma ambient during surface treatment prior to oxidation. Results of oxide electrical characterization are discussed in this chapter. A set of supplemental surface analysis experiments analyzed the conditioned SiC surfaces directly, without any subsequent oxide film growth. Surface metrology, addressed in chapters 4 and 5, consisted of non-contact C-KM depletion voltage transients for electrical evaluation of the surfaces, while XPS analysis served to provide additional chemical information. Thus the combined results from both oxide and semiconductor C-KM electrical characterization, as well as XPS chemical analysis, were drawn upon to discuss the impact of remote $(N_2{:}H_2)$* plasma surface conditioning on the afterglow oxidation mechanism, interfacial reactions, chemistry and structure regarding the important oxide/4H-SiC system.

A remote plasma processing approach, using selected variations of surface preparation, oxidation, and annealing steps, was used to prepare oxide thin films on n- and p-type epitaxial Si-face (0001) 4H-SiC 8° off-axis 3-in. wafers. All oxidations were performed in the remote plasma chemical reactor at 1 Torr total pressure as heated

substrates were exposed to a flow of rich oxidizing ($O_2$:$N_2O$:FG)* afterglow ambient described previously. The oxidation intervals used were 10−90 min. at temperatures 600°C−850°C, with resulting EOTs of 50−500 Å. Non-contact C-KM capacitance measurements were performed at multiple sites on each wafer to extract oxide electrical parameters and examine uniformity.

### 3.1. Oxidation time and temperature results vs. surface conditioning

In order to highlight the importance of initial surface chemistry, structure, and charge on subsequent oxide interface formation and growth mechanism, experiments were performed which incorporated remote plasma conditioning steps prior to afterglow oxide film growth. All surface treatment steps occurred at 600 °C for 20 min. duration in microwave-excited forming gas plasma (FG)* afterglow ambient containing reactive hydrogen and nitrogen species. For comparison, some processes included pre-oxidation exposures to the standard low-temperature ramp media, a non-excited $N_2$:$O_2$ 7:1 ambient, in order to simulate the same process temperature profile.

Figure 3.1 depicts electrical thickness values extracted from non-contact C-V curves obtained at multiple sites on both n- and p-type 4H-SiC epitaxial layers oxidized for various growth intervals at 850°C by afterglow of ($O_2$:$N_2O$:FG)* plasma discharge. Thickness values, determined by EOT extraction from $C_{ACC}$, were averaged over multiple points on each wafer. As witnessed in the figure, (FG)*-treated surfaces resulted in a growth rate increase, roughly 20%, during subsequent oxide film formation.

Clearly, the surface conditioning step in (FG)* afterglow has a significant influence on the initial oxide/4H-SiC interfacial reactions and afterglow oxidation mechanism. As

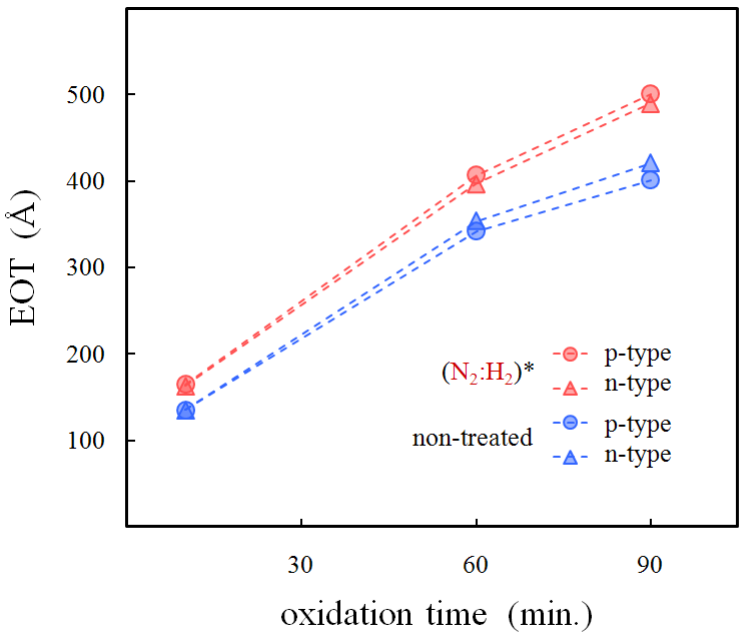


Figure 3.1. Electrical thicknesses of afterglow oxide films grown in ($O_2$:$N_2O$:FG)* afterglow ambient for various time intervals on 4H-SiC substrates at 850°C, some of which were subjected to (FG)* surface conditioning at 600°C. EOT is expressed as the average from multiple measurement sites. The oxide growth rate increased by roughly 20% when the SiC surface was remote plasma-treated prior to oxidation.

previously introduced, it was possible that the aggressive action of hydrogen species in the (FG)* afterglow media were responsible for removing residual contaminants following wet chemical cleaning. Hydrogen could also act to create a higher degree of order and passivation of the SiC surface, better suited for subsequent oxidizing reactions and interface formation. It was also possible that the excited and atomic nitrogen species within the (FG)* remote plasma ambient aided in formation of a thin nitrided overlayer or nitrogen-rich surface region which altered, chemically, mechanically, and electrically, the initial stages of afterglow oxidation. Nitrogen could act to remove or passivate C clusters in the surface layers, effectively reducing the presence of C-related surface defects and creating a Si-rich surface region. The removal of carbon from the surface region might

allow initial interfacial reactions to proceed at a faster rate, since the high-energy C-Si bond is an important factor contributing to the slow oxide growth rate on SiC.

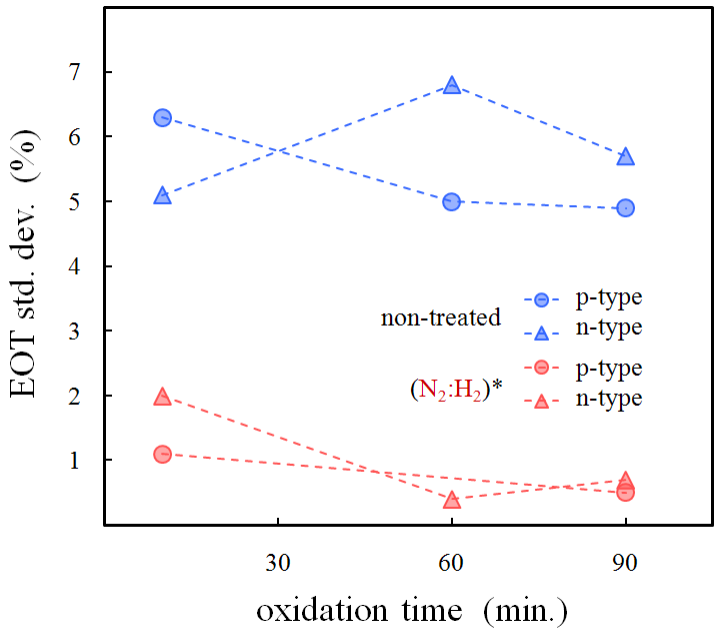


Figure 3.2. Thickness uniformity of afterglow oxide films grown for various time intervals on 4H-SiC substrates at 850°C, some of which were subjected to (FG)* surface conditioning at 600°C. The EOT standard deviation is expressed as a percentage of the average of EOT values from multiple measurement sites. EOT deviation decreased roughly five-fold when the SiC surface was remote plasma-treated prior to oxidation.

Another significant influence of the (FG)* surface conditioning step on the subsequent oxide interface formation and electrical properties was a stark improvement of oxide uniformity, both of EOT and $V_{FB}$ parameters. The SiC surfaces which were subjected to remote (FG)* plasma ambient prior to oxidation exhibited a much smaller degree of variation in their C-V characteristics obtained at multiple sites across the wafer. An example of this uniformity effect is given in figure 3.2, where the electrical thickness standard deviation is expressed as a percentage of the average EOT value from multiple measurement sites. The oxide/4H-SiC structures formed with (FG)* surface conditioning

prior to oxidation demonstrated a roughly five-fold reduction in thickness deviation. The observed uniformity improvement was suggested to result from the nitrogen and hydrogen reactive species helping to create a clean, smooth, and passivated SiC surface prior to oxidizing interfacial reactions, similar to previous studies which conditioned the surface prior to epitaxial growth [48–50]. These results illustrated the positive effects of the pre-oxidation (FG)* afterglow treatment on preparing the SiC surface for uniform oxide film formation.

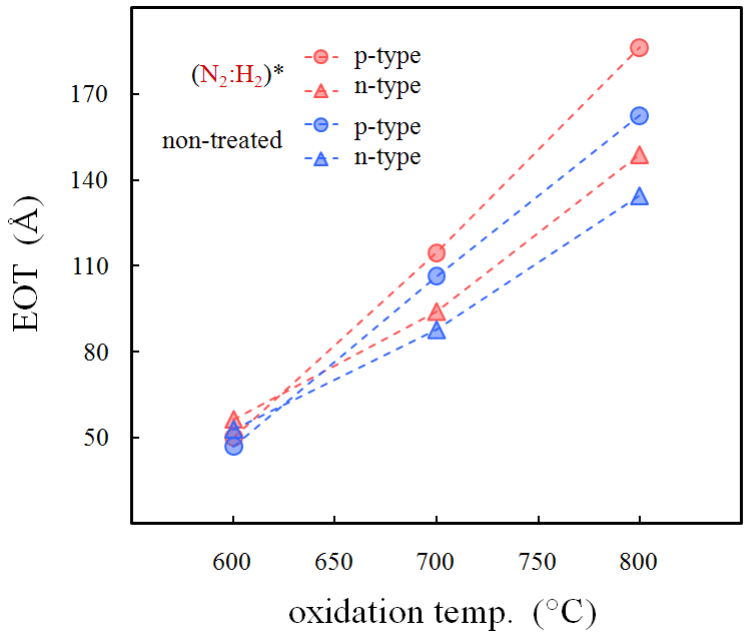


Figure 3.3. EOTs of afterglow oxide films grown for 15 min. on 4H-SiC substrates at temperatures between 600°C and 800°C, some of which were subjected to (FG)* surface conditioning at 600°C. EOT is expressed as the average over multiple measurement sites. The oxide growth rate increased by roughly 10-15% when the SiC surfaces were conditioned via (FG)* afterglow prior to oxidation.

Thus, pre-oxidation surface conditioning in $(N_2:H_2)$* afterglow facilitated an increase in oxide growth rate and improvement in film uniformity for various oxidation time intervals and film thicknesses at 850°C. Additional oxidations at temperatures other

than 850°C were required to examine the dependence of surface conditioning effects on oxidation temperature. A series of oxidations at temperatures 600°C−800°C were performed using ($O_2$:$N_2O$:FG)* remote plasma ambient for growth intervals of 15 min. Some 4H-SiC surfaces were conditioned by (FG)* afterglow for 20 min. at 600°C prior to film growth. As before, EOT values were extracted from non-contact C-KM capacitance curves, and averaged over multiple wafer sites. The oxide thickness results shown in figure 3.3 corresponded to approximately a 10-15% growth rate increase on both n- and p-type 4H-SiC substrates when the surfaces were conditioned by (FG)* remote-plasma before oxidation. Over the temperature range examined, the (FG)* surface conditioning effect on oxide film thickness was generally observed as a small increase in EOT. The magnitude of growth rate increase was observed to diminish at lower oxidation temperatures however, most noticeably at 600°C. This was somewhat misleading since the resulting oxide films grown for only 15 min. at this low temperature were extremely thin, around 50 Å in thickness. Hence, a roughly 10% growth rate increase translated to only a 5 Å difference in EOT.

A more detailed series of experiments were performed to examine the (FG)* afterglow conditioning effects at the relatively low oxidation temperature of 600°C. Films were grown during oxidation intervals of 15−60 min. in the standard ($O_2$:$N_2O$:FG)* remote-plasma chemistry. Some of the p-type 4H-SiC subtrates were conditioned for 20 min. in ($N_2$:$H_2$)* afterglow at 600°C preceding the oxidation stage. Average EOTs were extracted from C-KM capacitance measurements and are depicted in figure 3.4. The thickness results observed at 600°C were consistent with previous findings, although not as pronounced as the conditioning effects seen at 850°C oxidation temperatures. The

(FG)* afterglow conditioned 4H-SiC surfaces exhibited an increased film growth rate, roughly 10%, during subsequent oxidation intervals at 600°C.

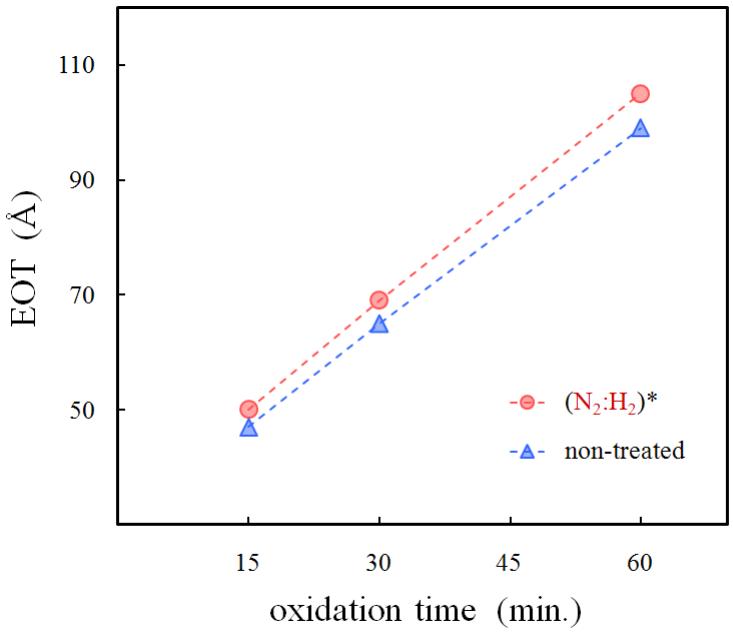


Figure 3.4. Electrical thicknesses of afterglow oxide films grown in ($O_2$:$N_2O$:FG)* afterglow ambient for various time intervals on p-type 4H-SiC substrates at 600°C, some of which were subjected to pre-oxidation (FG)* surface conditioning at 600°C. EOT is expressed as the average from multiple measurement sites. The oxide growth rate increased by roughly 10% when the SiC surface was remote plasma-treated prior to oxidation.

The uniformity of oxide film thickness was also examined for various oxidation time intervals at 600°C. The standard deviations of EOT values, expressed as percentages of the average oxide thickness obtained from multiple wafer sites, are visible in figure 3.5. Oxide films grown on afterglow-conditioned surfaces showed a slight decrease in thickness deviation, compared to oxides on RCA-treated surfaces. The observed improvement in oxide film uniformity was not nearly as significant as that found at 850°C oxidation temperature.

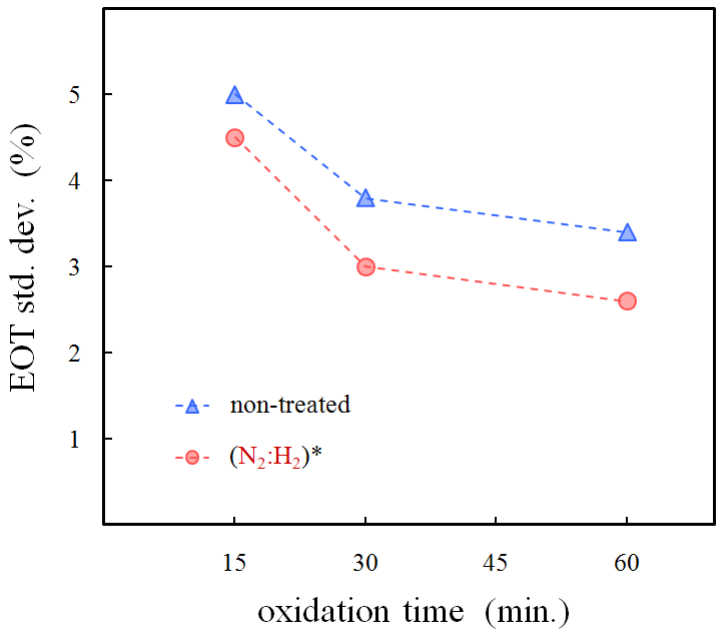


Figure 3.5. Thickness uniformity of afterglow oxide films grown for various time intervals on p-type 4H-SiC substrates at 600°C, some of which were subjected to pre-oxidation (FG)* surface conditioning at 600°C. The EOT standard deviation is expressed as a percentage of the average of EOT values over multiple measurement sites. EOT deviation showed a slight decrease when the SiC surface was remote plasma-treated prior to oxidation.

The action of reactive hydrogen and nitrogen afterglow chemistry on 4H-SiC surfaces thus resulted in a significant and positive impact on growth rate and film uniformity during subsequent oxidation for a wide variety of growth temperatures, time intervals, and oxide thicknesses. As determined by C-KM capacitance metrology, an increase in average film thickness and decrease in EOT deviation was observed when surfaces were conditioned via (FG)* remote plasma prior to the oxidation stage. These results were in agreement with the suggestion that $(N_2:H_2)$* afterglow exposure facilitated the preparation of a cleaner, smoother, ordered, passivated SiC surface with reduced surface defects and Si-enriched surface chemistry, compared to conventional wet chemical pre-furnace cleaning methods. Such a semiconductor surface was better suited

for *in-situ* oxide interface formation and film growth as part of a sequential afterglow processing approach. Additional electrical and chemical analysis of (FG)*-conditioned surfaces were needed to discuss these surface treatment effects in further detail (chapters 4 and 5).

## 3.2. High-temperature annealing effects vs. surface conditioning

Another figure of merit for examining the electrical behavior of oxide film structures was the flat-band voltage position of the C-V characteristic. $V_{FB}$ position was related to the net oxide charge and film thickness according to equation (23). Thus $V_{FB}$ gave an indication of the net total amount of charge incorporated into the oxide bulk and near-interfacial regions. It is desired that the flat-band position be stable under electrical stresses (device operation) and temperature stresses (post-oxidation processing). As shown in section 2.2.2, $V_{FB}$ shifting to larger magnitude values occurred during electrical testing of oxide/4H-SiC structures, and the $V_{FB}$ position saturated to a maximum value after strong accumulation of the semiconductor. A consistent measurement protocol was implemented, in which this max $V_{FB}$ position was used for comparing C-V characteristics of different films and processes.

It was of particular interest to examine the stability of $V_{FB}$ position during high-temperature inert annealing of oxide films. The purpose of such anneals was to mimic the temperature stresses involved during typical post-oxidation processing such as poly-silicon gate annealing or silicide formation. Based on preliminary findings, it seemed possible that pre-oxidation afterglow surface conditioning might have an impact on $V_{FB}$ shifting behavior during post-oxidation annealing at high temperature. However, these results were inconclusive since they were drawn from a scattering of experiments

performed at different times, with differing conditions such as ramp media, load and unload temperature, oxidation time, etc. This of course warranted a specific and consistent series of experiments to investigate the $V_{FB}$ response to high-temperature post-oxidation annealing, as a function of surface conditioning.

Afterglow oxidations were performed at both 600°C and 850°C in standard ($O_2$:$N_2O$:FG)* media. At 600°C the 4H-SiC substrates were oxidized for 60 min. followed by optional Ar annealing at 950°C for 30 min. At 850°C the oxidation interval was 15 min. followed by an optional 30 min. Ar anneal at 1000°C after furnace ramp-up. Preceding the oxidation stage, semiconductor surfaces were conditioned for 20 min. at 600°C in forming gas ($N_2$:$H_2$)* 19:1 remote-plasma afterglow chemistry or non-excited $N_2$:$O_2$ 7:1 media. The resulting C-V characteristics obtained by non-contact corona-Kelvin metrology are displayed in figures 3.6 and 3.7 for 850°C and 600°C oxidation temperatures, respectively.

From the $V_{FB}$ shifting behavior observed, it was apparent that high-temperature annealing did have a significant, yet undesirable, impact on flat-band position. All oxide films which underwent post-oxidation Ar annealing exhibited C-V curves with larger $V_{FB}$ magnitudes compared to non-annealed films. This corresponded to more negative $V_{FB}$ values on p-type and more positive values on n-type SiC. The increase in flat-band voltage implied that high-temperature stress leads to defect formation and charge incorporation, and thus a higher amount of net oxide charge, $Q_{TOT}$. The general effect of $V_{FB}$ increase after annealing seemed to have little dependence on surface conditioning or oxidation temperature.

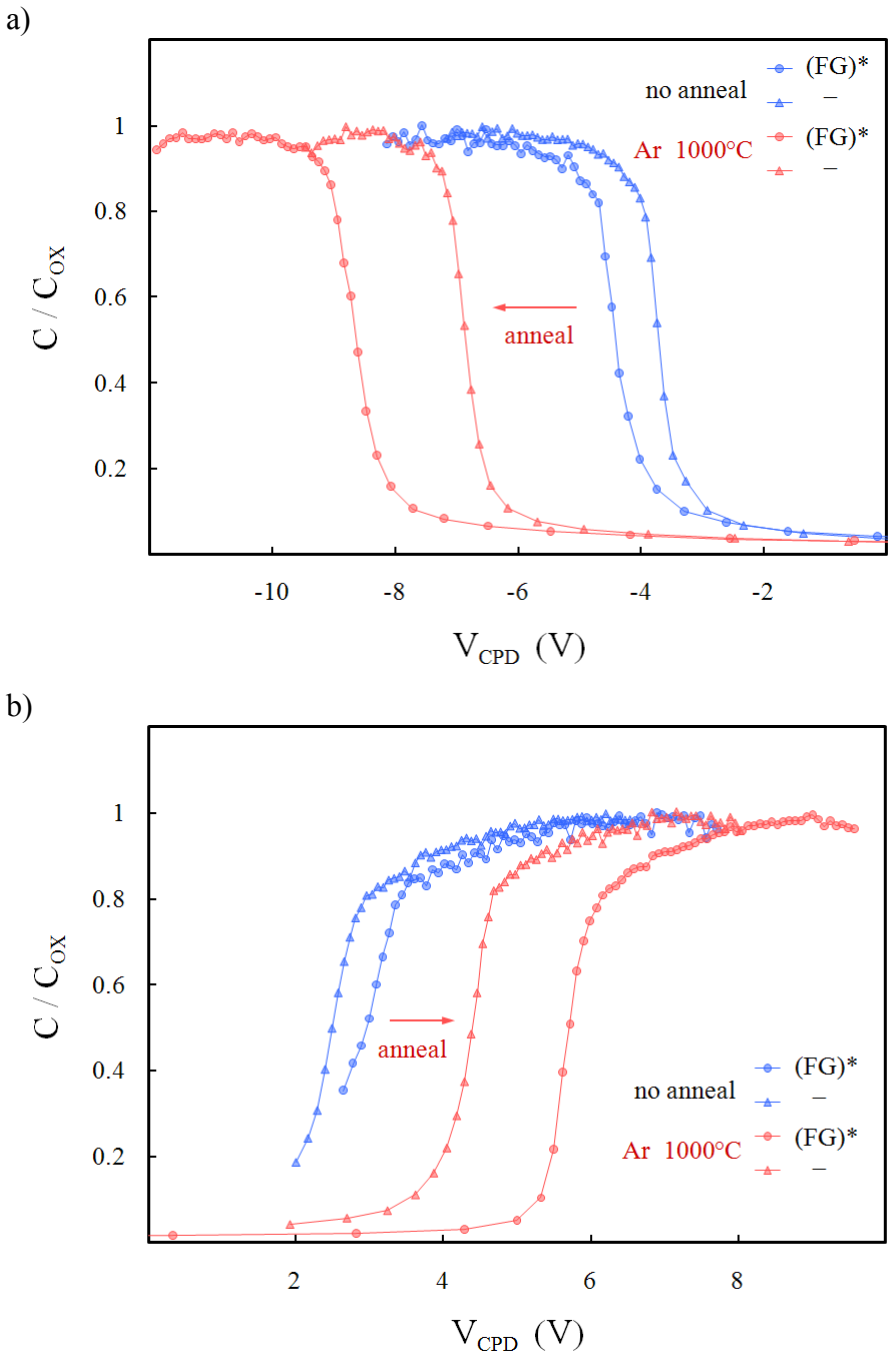


Figure 3.6. Non-contact C-V characteristics of oxide films grown for 15 min. at 850°C on p-type (a) and n-type (b) 4H-SiC substrates, some of which underwent pre-oxidation (FG)* surface conditioning at 600°C and/or post-oxidation Ar annealing at 1000°C for 30 min. All annealed films demonstrated significant $V_{FB}$ shifting to larger magnitude values. Also, films grown on (FG)*-treated surfaces demonstrated slightly larger $V_{FB}$ values.

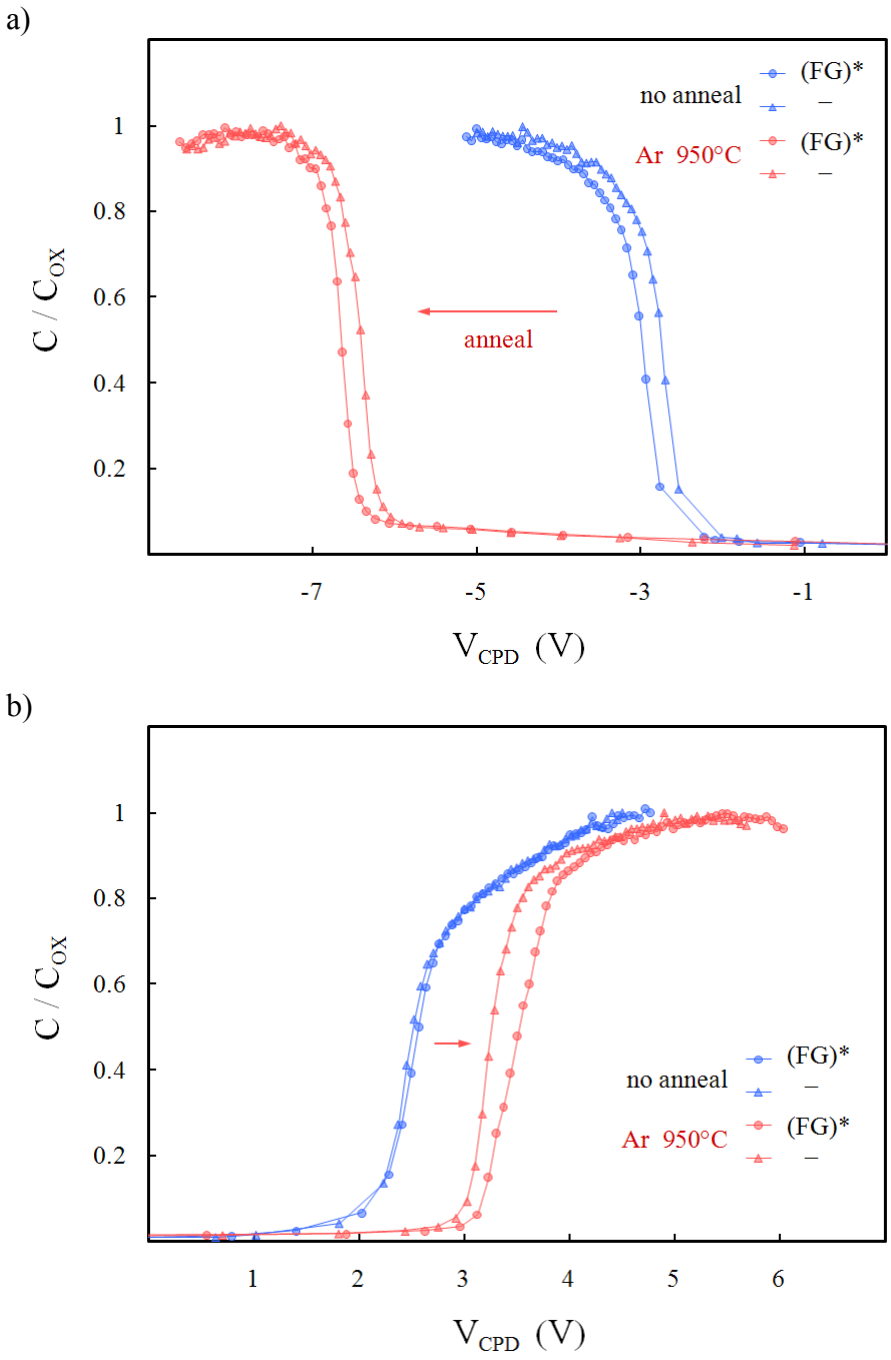


Figure 3.7. Non-contact C-V characteristics of oxide films grown for 60 min. at 600°C on p-type (a) and n-type (b) 4H-SiC substrates, some of which underwent pre-oxidation (FG)* surface conditioning at 600°C and/or post-oxidation Ar annealing at 950°C for 30 min. All annealed films demonstrated significant $V_{FB}$ shifting to larger magnitude values. Also, films grown on (FG)*-treated surfaces demonstrated slightly larger $V_{FB}$ values.

It should be noted that when surfaces were treated by (FG)* afterglow before oxidation, the resulting $V_{FB}$ was slightly larger compared to films grown on non-treated surfaces. This effect was visible at both 600°C and 850°C oxidation temperatures and for both annealed and as-grown films. Also, the absolute value of $V_{FB}$ and the magnitude of shifting after anneal were both smaller on n-type than p-type samples, which is a general property of all our afterglow oxide films on 4H-SiC. Furthermore, $V_{FB}$ magnitudes and shifts after annealing were slightly smaller for films grown at 600°C compared to 850°C.

Oxide film thickness variations between experiments can account at least partially for some of these observations. At each growth temperature, the film thicknesses from different experiments were similar, but not identical. Due to this variation in EOT between experiments, there was a corresponding variation in oxide capacitance, which was inversely proportional to thickness per equation (21). The capacitance curves in the figures have been plotted normalized to $C_{OX}$ for ease of viewing. However, $V_{FB}$ position was also thickness-dependent. For a fixed level of $Q_{TOT}$, a thicker oxide film corresponds to a smaller $C_{OX}$ and hence a larger $V_{FB}$ per equation (23).

As discussed in section 3.1, films grown on (FG)*-conditioned surfaces were slightly thicker. This result was consistent with the increased $V_{FB}$ observed on afterglow-treated surfaces. Likewise, the oxides grown at 850°C were thicker than those formed at 600°C, which was also consistent with the larger absolute values and shifts of $V_{FB}$ observed in films grown at the higher temperature.

Film thickness variations were not the sole cause of changes in $V_{FB}$ position. The other contributing factor was the net total oxide charge mentioned previously. Simple estimates of $Q_{TOT}$ were calculated from the C-V measurements using $C_{ACC}$ and $V_{FB}$ values,

Table 3.1. Net total oxide charge estimated from non-contact C-V characteristics of afterglow oxide films. Post-oxidation high-temperature Ar annealing caused a significant increase in $Q_{TOT}$, regardless of pre-oxidation surface conditioning or oxidation temperature.

| $Q_{TOT}$ ($\times 10^{12}$ cm$^{-2}$) | | p-type 4H-SiC | | n-type 4H-SiC | |
|---|---|---|---|---|---|
| | | $T_{OX}$ = 850°C | $T_{OX}$ = 600°C | $T_{OX}$ = 850°C | $T_{OX}$ = 600°C |
| no anneal | $(N_2:H_2)$* | 6.7 | 6.6 | 4.5 | 4.9 |
| | — | 6.2 | 6.4 | 4.4 | 5.2 |
| anneal Ar | $(N_2:H_2)$* | 12 | 12 | 7.4 | 7.1 |
| | — | 11 | 13 | 7.0 | 6.8 |

and are listed in table 3.1. These $Q_{TOT}$ estimates took into account any thickness variations. By far the most evident trend was the increase in $Q_{TOT}$ caused by high-temperature Ar annealing of oxide films. This was consistent with the $V_{FB}$ shifting to larger values during annealing. Also, the oxides on n-type material had somewhat smaller $Q_{TOT}$ compared to p-type, which was consistent with the smaller $V_{FB}$ values generally exhibited by films on n-type compared to p-type 4H-SiC. On the contrary, both pre-oxidation surface treatment and choice of oxidation temperature seemed to have very little observable impact on $Q_{TOT}$.

Based on these results, it was concluded that the effects of conditioning 4H-SiC surfaces in $(N_2:H_2)$* afterglow chemistry did not have a significant impact on oxide charge incorporation during oxidation and annealing processes. Furthermore, high-temperature post-oxidation annealing did cause a significant increase in $V_{FB}$ and $Q_{TOT}$ values compared to as-grown dielectric films. The observed oxide charge increase might have resulted from interfacial rearrangement and viscous oxide flow at the elevated annealing temperatures. Despite posing a challenging hurdle to the development of 4H-

SiC device processing and manufacture, this problem did not seem to be closely related to the focus on surface conditioning effects in afterglow oxidation processing, and did not warrant further discussion within the scope of this work. Hence, the issue of $V_{FB}$ shifting during high-temperature annealing remains to be addressed in future work.

A variety of afterglow oxidation experiments were performed on 4H-SiC at growth temperatures of 600°C−850°C for 10−90 min. intervals resulting in oxide films 50−500 Å thick. An emphasis was placed on the effects of surface conditioning via $(N_2{:}H_2)$* afterglow to prepare the substrate for oxidation. Corona-Kelvin capacitance metrology was used to evaluate electrical oxide parameters. General trends of growth rate increase and film uniformity improvement were witnessed to be caused by pre-oxidation (FG)* surface treatment. Tentative hypotheses of cleaning, nitridation, surface passivation, defect reduction, and carbon removal were suggested as mechanisms to explain the observed effects of hydrogen and nitrogen species on the surfaces. The following chapters treat a deeper investigation of conditioned 4H-SiC surfaces, in which the metrology tools of C-KM depletion $V_{CPD}$ transient characterization and XPS analysis were used to supply additional electrical and chemical evaluation of surface treatments.

# Chapter 4. Corona-Kelvin $V_{CPD}$ Transients on Conditioned 4H-SiC Surfaces

Afterglow conditioning and other surface treatments on 4H-SiC were investigated in an attempt to further understand the impact of (FG)* exposure as a pre-oxidation surface preparation technique. Non-contact $V_{CPD}$ voltage transient measurements were used to provide important and direct electrical information regarding surface barrier and charge compensation processes after depletion of a bare semiconductor by corona charge deposition. Corona-Kelvin depletion voltage monitoring was used as a non-contact method for electrical evaluation of 4H-SiC surfaces after various conditioning treatments. A measurement protocol was established and the $V_{CPD}$ voltage decays on depleted 4H-SiC surfaces were interpreted in terms of a charge compensation model. Forming gas (FG)* afterglow treatments were compared with other selected types of surface conditioning. Treatment time and temperature were addressed, as well as the durative stability of conditioned surfaces in retaining their state following treatment.

## 4.1. $V_{CPD}$ transient measurement protocol and interpretation

The chosen method for electrical characterization of semiconductor surfaces in this work combined corona charge deposition and non-contact voltage measurement, as with the oxide film characterization discussed previously. However, in the case of the bare semiconductor, a single corona charge pulse was deposited on the surface. A large corona dose and appropriate charge polarity were chosen in order to achieve strong depletion of the semiconductor. Following charge deposition, the depletion voltage was

observed over a significant time interval. The first $V_{CPD}$ reading was executed almost immediately after the corona charge pulse, delayed by approximately one second while the CPD probe was shifted to the deposition site. Without subsequent charging steps, the $V_{CPD}$ decayed in magnitude from the first measured value.

Recalling equation (27), in the absence of an oxide layer, and neglecting the miniscule constant $\Phi_{MS}$ (< 1V), the measured depletion voltage was practically equivalent to the semiconductor surface potential barrier:

$$V_{CPD} \approx V_{SB} \tag{29}$$

Thus the observed $V_{CPD}$ transient corresponded to a decay of the depletion surface barrier from its initial value following the corona charge pulse. The $V_{SB}$ decay was associated with charge compensation processes in the semiconductor. In particular, some means of carrier generation/emission and transport allowed $V_{CPD}$ to change after the initial space-charge region width and surface barrier voltage were established following corona application.

The basic $V_{CPD}$ transient measurement protocol is summarized in the following two sequential steps:

1) deposit large corona charge pulse to force semiconductor into strong depletion.

2) monitor $V_{CPD}$ over time as the surface barrier decays from its initial value.

For all $V_{CPD}$ transient metrology described in this work, a standard corona pulse size was consistently used to achieve an areal density of $Q_C = 1.5\times10^{12}$ q cm$^{-2}$, or equivalently $2.4\times10^{-7}$ C cm$^{-2}$, on the measurement site. Corona ions, $CO_3^-$ or $H_3O^+(H_2O)_n$ , were deposited on n- or p-type SiC material, respectively, appropriate for depleting the semiconductor. Following the initial $V_{CPD}$ measurement ($V_0$), the voltage was continually

monitored over time as additional readings were repeated every 200 ms for a total interval of 180 s. Thus each voltage curve was comprised of 900 data points obtained during a full 3 minutes after charge deposition.

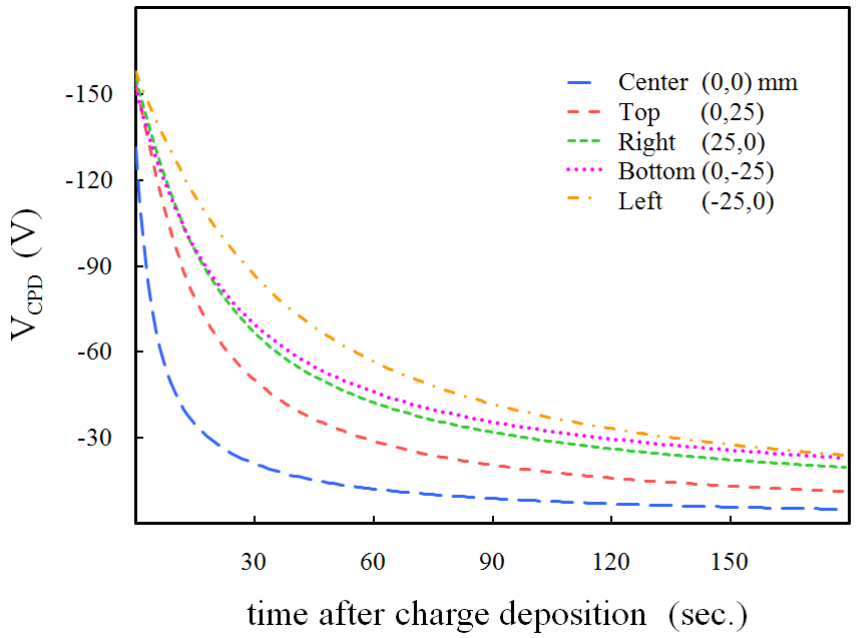


Figure 4.1. Depletion surface barrier transients obtained at multiple sites on RCA cleaned n-type 4H-SiC epi-wafer A after negative corona deposition. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Decay of $V_{SB}$ and depletion region width was attributed to charge compensation processes due to carrier emission from traps in the presence of high electric field.

As an example, consider the $V_{CPD}$ decay curves depicted in figure 4.1. The SiC material examined was the Si-face of an n-type ($N_d = 1\times10^{15}$ cm$^{-3}$) 4H-SiC 8° off-axis 3-in. epi-wafer obtained from Cree, Inc. and grown with their standard epitaxial process. This epitaxial wafer was identified as wafer "A". Prior to measurement, the SiC surface was only processed by wet cleaning using standard piranha and RCA solutions and ending with a dilute HF dip and DI rinse. $V_{CPD}$ transients were obtained at 5 different wafer sites, organized in a cross pattern with radius 25 mm, and referenced to the major

flat as the bottom direction on the wafer. Some small variation in starting value ($V_0$), final value ($V_{sat}$), and decay rate ($\Delta V_{CPD}$) were observed over wafer A (figure 4.1). However, the general trend of $V_{CPD}$ decay was clearly evident. The first measured value of depletion surface potential barrier was around an average of $V_0 = -150$ V, and slowly decayed during 3 minutes to an average of −16 V.

The observed temporal decay of $V_{SB}$ was associated with a corresponding decrease in space-charge region width, proportional to the square root of the surface barrier:

$$W^2 = 2\varepsilon_0\varepsilon_r V_{SB}(qN_d)^{-1} \tag{30}$$

where W is depletion region width, $\varepsilon_0$ is permittivity of vacuum, $\varepsilon_r$ is relative permittivity of the semiconductor, $V_{SB}$ is surface potential barrier, q is elemental charge, and $N_d$ is dopant concentration. The space-charge density $Q_{SC}$ was directly proportional to the depletion region width:

$$Q_{SC} = qN_dW \tag{31}$$

and the maximum value of $Q_{SC}$ must equal the surface corona charge density $Q_C$ minus any compensating charge generated in the semiconductor. After the space-charge region and surface barrier were initially established, associated with the deposition of corona charge on the semiconductor surface, any decay in $V_{SB}$ and W was due to the emission/generation and transport of charge carriers resulting in the compensation of surface corona charge. Otherwise, electrostatic equilibrium would remain unperturbed, resulting in a constant surface barrier. Given the fact that these measurements were performed at room temperature, and in ambient darkness, direct band-to-band carrier generation was highly improbable due to the large band-gap of 3.27 eV. It was similarly

improbable that electron-hole pair generation assisted by mid-gap generation centers was a dominating factor.

The principal mechanism of temporal charge compensation was suggested to revolve around the emission of charge carriers from deep-level traps concentrated in the semiconductor surface region. As majority carriers were emitted from traps into the conduction or valence energy bands (n- or p-doped, respectively) they were swept into the semiconductor, driven by the electric field present at the surface, and eventually recombined with dopant ions in the space-charge region. The release and movement of majority charge away from the surface was responsible for compensation of corona surface charge, and thus the observed decay of surface potential barrier height and corresponding depletion region width shrinkage.

The proposed charge compensation mechanism is simply depicted in figure 4.2 by way of two snapshot diagrams. In the illustration, a dose of negative corona charge was deposited on an n-type SiC surface, which repelled majority carriers (electrons) into the semiconductor. Due to the surface electric field penetrating into the semiconductor, a space-charge region of positively ionized dopant atoms was established (figure 4.2a) with a corresponding depletion charge density $Q_{SC}$ and surface barrier voltage $V_{SB}$. However, the probability of carrier emission from traps in the surface region was also enhanced by the electric field. Any emitted electrons were driven into the semiconductor by the surface E field and recombined with dopant ions in the space-charge region. Regardless of whether the filled traps were neutral or charged impurities, the emission of electrons resulted in a net positive charge increase in the surface region and compensation of negative surface corona charge. Consequently, the depletion region width, space-charge

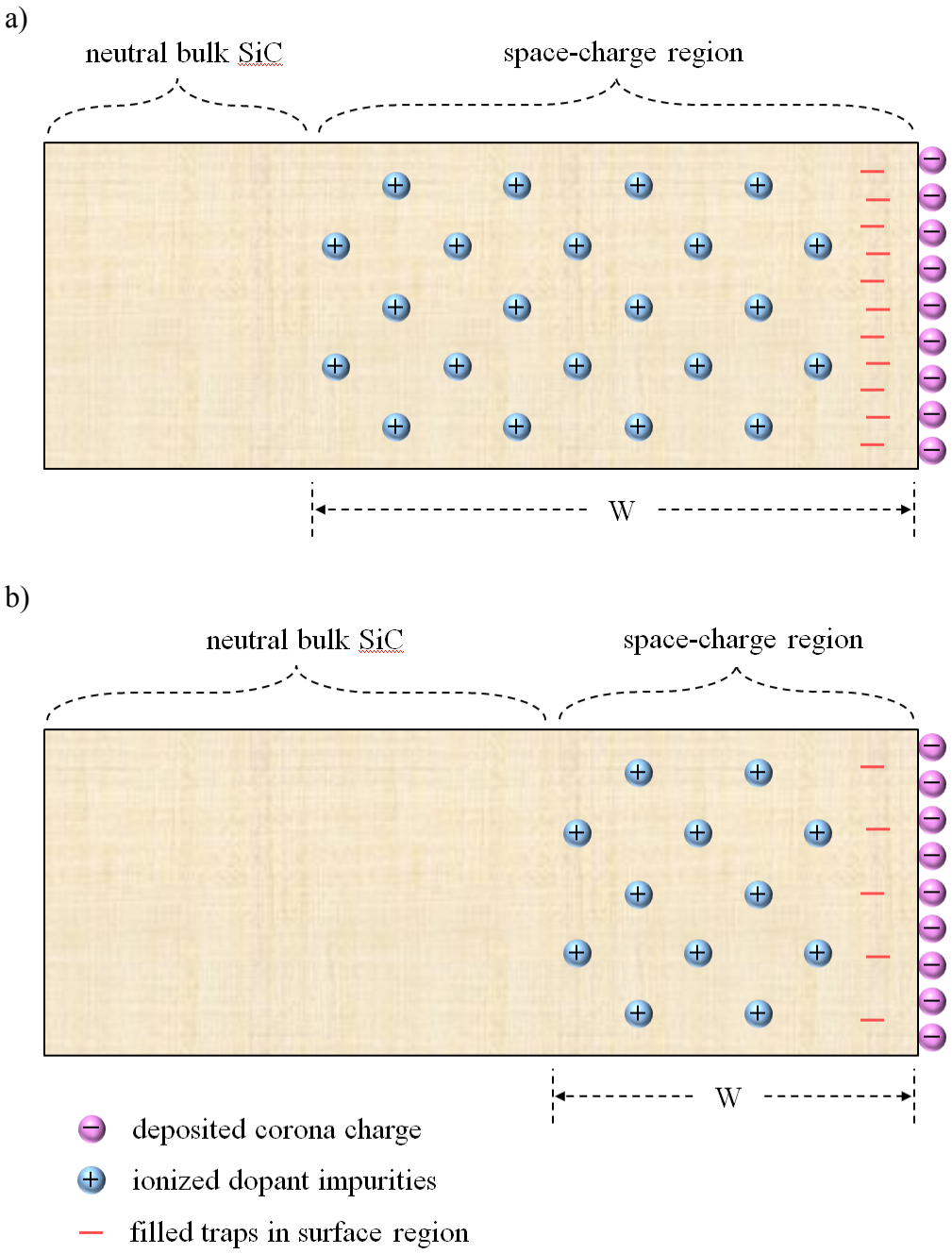


Figure 4.2. Diagram of the charge compensation mechanism associated with the temporal decay of surface barrier, depletion width, and space-charge density. Field-enhanced carrier emission from surface traps and recombination with dopant ions in the space-charge region result in the compensation of surface corona charge. The depletion region width and surface barrier decay from their initial values established at corona deposition (a) to smaller values after charge emission from surface traps (b).

density, and surface potential barrier decreased in order to maintain charge neutrality (figure 4.2b).

Without considering the input of carrier emission from traps, the depletion space-charge density equaled the deposited corona charge. However, because of charge emission processes, the space-charge deviated from the ideal according to:

$$Q_{SC} = Q_C - Q_{def} \quad (32)$$

where $Q_{SC}$ is depletion space-charge density, $Q_C$ is surface corona charge density, and $Q_{def}$ is the effective density of compensating charge liberated from defects over time.

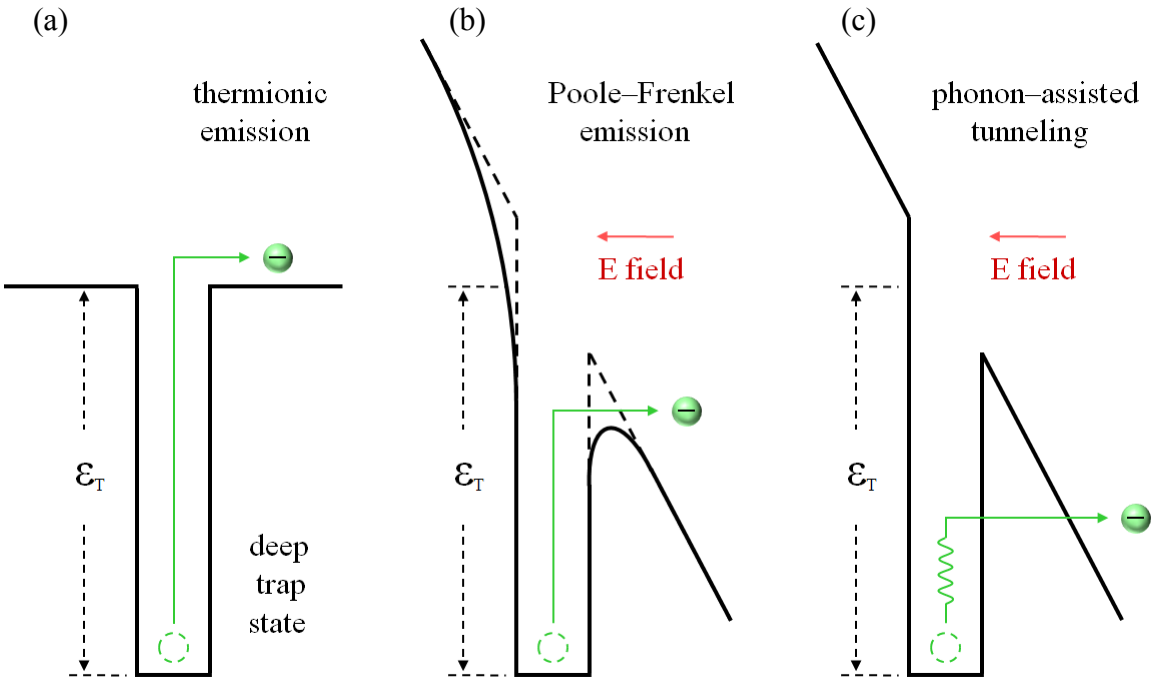


Figure 4.3. Illustration of electric field enhanced carrier emission from localized states. In the presence of electric field, Poole-Frenkel emission (b) or phonon-assisted tunneling mechanisms (c) can increase the probability of carrier emission compared to the basic thermionic emission of carriers without E field stimulation (a) [65].

Thus the observed decay in the surface potential barrier was suggested to be a result of charge compensation from field-stimulated carrier emission processes. In the absence

of electric field, carriers may be emitted from traps by thermionic emission (figure 4.3a), using only thermal energy from the environment to provide the difference between the trap level and conduction band ($\varepsilon_T$). However, thermionic emission was improbable to occur at room temperature from deep levels with $\varepsilon_T >> kT \approx 25mV$, since the probability of emission had an inverse exponential dependence on trap energy normalized to thermal ambient energy:

$$r_e \sim \exp(-\varepsilon_T / kT) \tag{33}$$

where $r_e$ is emission rate, $\varepsilon_T$ is relative trap energy, and kT is thermal energy.

In an electric field, carrier emission from traps may be enhanced in two ways. The first mechanism, known as Poole-Frenkel emission [66], occurs due to Coulomb barrier lowering in the presence of an electric field (figure 4.3b). Poole-Frenkel emission processes are only possible when the filled trap is in a charged state, because barrier lowering does not occur if the defect is neutral. Also, Poole-Frenkel emission is significant at relatively low electric fields. At higher E field strengths, phonon-assisted tunneling becomes the more dominant emission mechanism (figure 4.3c) [65]. The enhanced degree of energy band-bending at high fields allows carriers to tunnel from the trap level directly into the conduction band with non-negligible probability. When partially assisted by energy input from thermal vibrations, the probability of tunneling increases because the energy barrier that the electron must tunnel through is less.

The surface electric fields resulting from corona ion deposition in $V_{CPD}$ transient metrology were relatively high. The standard corona dose of $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$ corresponded to an electric field of 269 kV/cm at the surface, according to the relation:

$$E = Q_C / \varepsilon_0 \varepsilon_r \quad (34)$$

Regarding the transition between phonon-assisted tunneling and Poole-Frenkel emission as competing processes, values below the order of 1 kV/cm were considered to lie within the low-field regime [65]. Hence, the field strengths typically used in this work (hundreds of kV/cm) warrant the conclusion that phonon-assisted tunneling was the more dominant mechanism for field-stimulated carrier emission. Thus, the observed temporal decay of surface potential barrier in depletion was suggested to be a result of charge compensation due to field-enhanced carrier emission from deep-level surface traps.

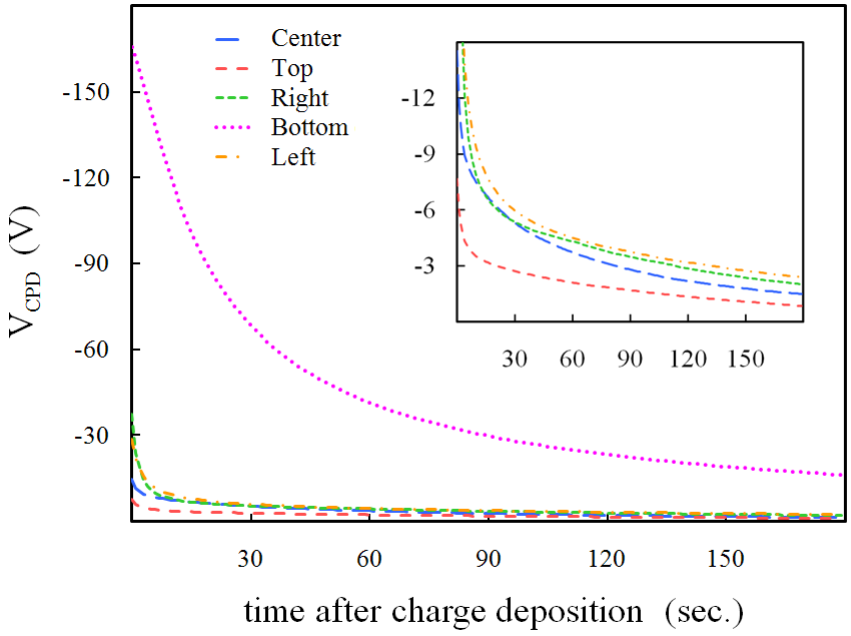


Figure 4.4. Depletion surface barrier transients obtained at multiple sites on RCA cleaned n-type 4H-SiC epi-wafer B after negative corona deposition. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. The inset is zoomed in on the low-voltage portion of curves. The variation of initial measured voltage $V_0$ and the faster rates of $V_{SB}$ decay indicated higher concentrations of charge-emitting defects and non-uniform epitaxial quality on wafer B compared to wafer A (see figure 4.1).

Defect concentration variations, particularly near the SiC surface, were expected to have an observable impact on $V_{CPD}$ transient behavior. Shallow states ($\varepsilon_T < kT$) were suggested to empty immediately following corona deposition, much faster than the initial voltage reading $V_0$. Deep-level traps were expected to contribute to the slow $V_{SB}$ decay observable over the 3 min. transient measurement. Thus, both the initial voltage and rate of surface barrier decay depended on defect levels and concentrations in the semiconductor surface region.

Figure 4.4 shows voltage decays obtained on another n-type 4H-SiC epi-layer, identified as wafer "B", which was grown with a non-standard epitaxial process by Cree, Inc and doped identical to wafer A ($N_d = 1\times10^{15}$ cm$^{-3}$). In comparison to material A, epi B had higher defect levels and more variation of defect concentrations across the wafer. This was clearly evident when comparing the $V_{CPD}$ decay behavior between figures 4.1 and 4.4. On average, wafer B demonstrated much lower initial $V_0$ readings, and much faster rates of $V_{CPD}$ decay, than the standard epitaxial material A. However, the bottom measurement point (0,−25mm) on B had a high $V_0$ and slow $V_{SB}$ decay, indicating a high degree of non-uniformity of charge-emitting defects across the wafer. In fact, the bottom of wafer B behaved comparably to the best points on A. In general, the $V_{CPD}$ transient was fairly uniform across wafer A. The center point demonstrated the largest deviation from the other wafer sites. The faster voltage decay in the center implied higher concentrations of deep-level charge-emitting traps compared to the radial sites near the outside of the wafer.

The majority of $V_{CPD}$ transient data presented in this work consisted of a single decay curve obtained immediately following the initial corona charge pulse deposited on

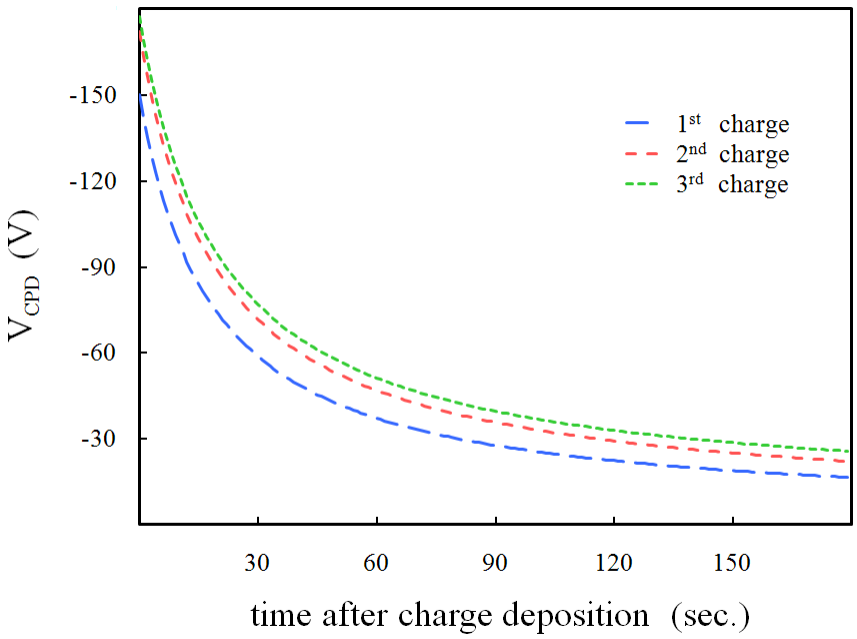


Figure 4.5. $V_{CPD}$ transient decays with consecutive repetitions of corona deposition spaced at 3 min. intervals, obtained on RCA cleaned n-type 4H-SiC epi-wafer A. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following each of 3 corona applications of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. The rate of $V_{SB}$ decay was very consistent among repeated measurements.

a freshly treated surface. However, similar transient behavior was observed with additional charge pulses and voltage measurements. Figure 4.5 gives an example of consecutive charge and decay measurements on wafer A after an RCA clean. Each curve in the figure was the average of transients from multiple wafer sites. Three separate corona pulses of $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$ were spaced at intervals of 3 minutes, and the $V_{CPD}$ decays were recorded after each deposition. The average rates of decay and starting values were quite similar. A very slight voltage increase was observed at each subsequent measurement. Although most of the depletion space-charge had dissipated due to charge compensation during the 3 min. of measurement, some small quantity of

space-charge still remained when the next corona pulse and measurement were executed. Thus the depletion region width was slightly larger after the next corona deposition.

## 4.2. Surface conditioning impact on $V_{CPD}$ decay

The observed slow $V_{CPD}$ decay after depletion charging was suggested to result from carrier emission from surface deep-level traps, recombination with depletion region space-charge, and compensation of surface corona charge. As previously introduced, defects in the 4H-SiC surface region were attributed to a conglomeration of various dangling bonds, chemical states, hydrocarbons, vacancies, C-clusters, other C-related defects, hydroxyls, oxygen, fluorine and other residual contaminants, etc. Hence, $V_{SB}$ transient decay behavior was used as an indication regarding concentrations of charge-emitting surface defects, and served as a valuable figure of merit when comparing the effectiveness of different surface conditioning treatments in the reduction and passivation of surface defects.

A series of surface conditioning experiments were performed to compare the standard pre-oxidation (FG)* afterglow treatment with other conditioning treatments. The baseline afterglow treatment consisted of an RCA clean, furnace loading, temperature ramp-up in $N_2$:$O_2$ 7:1, 20 min. of exposure to ($N_2$:$H_2$)* 19:1 afterglow at 600°C, followed by immediate unloading, cooling, and characterization of the treated surface. Other treatment ambients included 20 min. exposures to pure ($N_2$)* afterglow or non-excited $N_2$:$O_2$ 7:1 media at 600°C. Surfaces rinsed in DI water following the baseline (FG)* afterglow conditioning were also examined, as well as the previously introduced RCA cleaned surfaces.

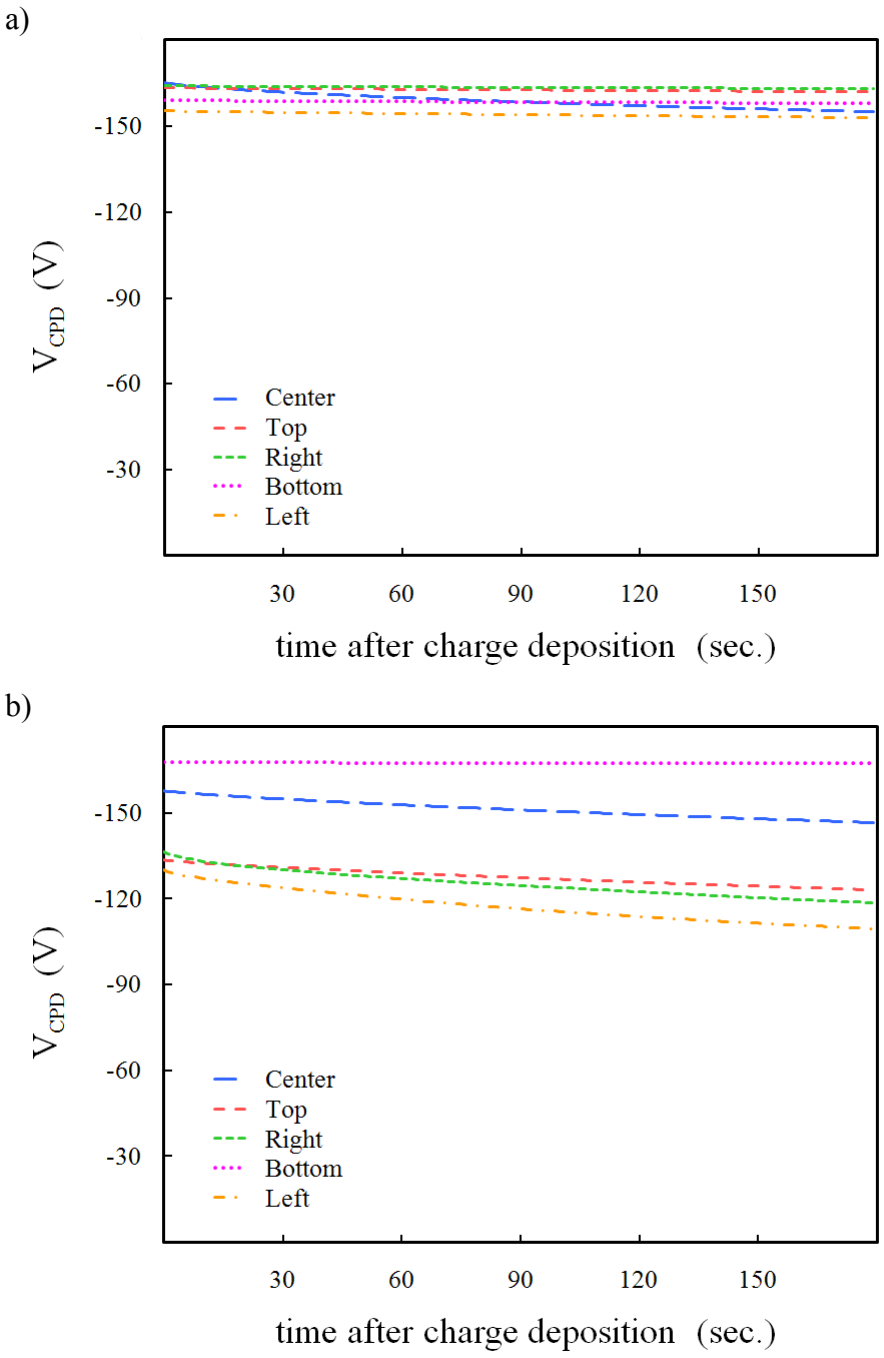


Figure 4.6. Depletion $V_{SB}$ transients obtained at multiple sites on n-type 4H-SiC epi-wafers A (a) and B (b) following $(N_2{:}H_2)$* afterglow surface conditioning for 20 min. at 600°C. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C$ = $2.4\times10^{-7}$ C $cm^{-2}$. Rates of $V_{SB}$ decay were extremely slow, implying a much smaller concentration of charge-emitting surface defects on (FG)*-treated surfaces vs. RCA clean (compare to figures 4.1, 4.4 for wafers A, B).

Depletion voltage decays on epi-layers A (figure 4.6a) and B (figure 4.6b) were obtained after the baseline (FG)* afterglow treatment for 20 min. at 600°C. The $V_{CPD}$ transient response on (FG)*-conditioned surfaces was dramatically improved in comparison to the same materials after RCA cleaning (figures 4.1, 4.4). An extremely slow rate of $V_{SB}$ decay was observed on the standard epi-wafer A. Averaged across the multiple wafer sites, the initial $V_{CPD}$ value around −161V decayed an average of only 3V during the 3 min. measurement interval. The drastic reduction in surface barrier decay rate implied very few sources of compensating charge that were evident during the measurement, attributed to lower levels of deep-level traps on the surfaces prepared via the (FG)* afterglow baseline process. Although a comparatively faster rate of decay occurred in the center point, this was consistent with the observed decays after RCA cleaning, which indicated that the center of wafer A had higher concentrations of charge-compensating defects relative to the other measurement sites.

However, an ideal surface barrier around –200V was expected if all the corona charge were perfectly imaged in the space-charge region. The measured $V_0$ value of −161V corresponded to roughly $2.5\times10^{-8}$ C $cm^{-2}$ of compensating charge density emitted after corona depostion but before initial $V_{CPD}$ measurement. The majority of this initial charge compensation was attributed to shallow trap levels and crystal defects, and were not strongly affected by surface condition.

The $V_{CPD}$ decays observed on wafer B after (FG)* conditioning were also somewhat faster compared to wafer A. An average of 12V of decay over 3 min. was observed on wafer B, compared to 3V on wafer A. The faster decay rates and larger voltage distribution were also consistent with the RCA clean results, implicating the presence of

higher surface defect concentrations and non-uniform epitaxial quality on wafer B. The bottom point on wafer B exhibited very slow decay, only 0.3V during 3 min. of transient measurement. This was slower than even the best points on wafer A, which decayed 0.9V and 1.0V over 3 min. It was concluded that the wafer B bottom point had extremely low concentrations of surface defect sources for charge compensation, while the rest of the tested wafer areas had higher surface defect densities.

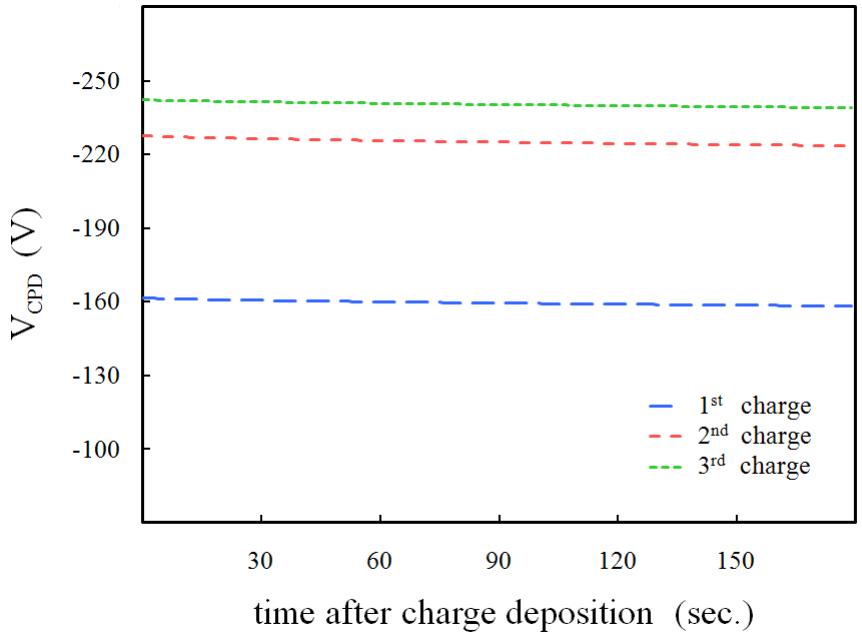


Figure 4.7. $V_{CPD}$ transient decays with consecutive repetitions of corona deposition spaced at 3 min. intervals, obtained on n-type 4H-SiC epi-wafer A after (FG)* surface treatment for 20 min. at 600°C. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following each of 3 corona applications of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Rate of $V_{SB}$ decay was very consistent among repeated measurements, while the increase in initial measured voltage $V_0$ after each consecutive corona deposition was due to remaining depletion space-charge from previous measurement.

The results of repeated $V_{CPD}$ transient measurements on (FG)*-conditioned surfaces are shown in figure 4.7 as averages of multiple sites on wafer A. Three consecutive charge and decay intervals were executed. After each consecutive charge pulse, the rates

of voltage decay were similar. However, the starting $V_{CPD}$ value increased significantly, reaching a $V_0$ of −242V after the 3rd charging. Due to the slow rate of $V_{SB}$ decay on the (FG)*-treated surfaces, much of the depletion space-charge remained at the end of the 3 min. measurement interval. The subsequent deposition of another corona pulse caused an increase in space-charge density and depletion region width, resulting in a higher $V_{SB}$ value at the beginning of the next transient. The increase in $V_0$ upon subsequent measurements was not nearly as dramatic on the RCA cleaned surfaces (figure 4.5) because of the much higher rates of $V_{SB}$ decay due to higher concentrations of charge-emitting surface defects.

Evidently, a large reduction of surface charge-emitting defects was accomplished by conditioning of 4H-SiC surfaces in $(N_2{:}H_2)$* afterglow, as supported by a large decrease in depletion $V_{SB}$ decay rate relative to RCA cleaned surfaces. Other treatments were examined to compare to the standard (FG)* conditioning process. $V_{CPD}$ transient measurements were obtained on wafer A (figure 4.8a) and wafer B (figure 4.8b) after each treatment. Curves shown are averages from multiple wafer sites.

For ease of visualization, the same results are shown in figure 4.9 with voltage values plotted relative to the initial $V_{CPD}$ reading, as:

$$\Delta V_{CPD} = V_{CPD} - V_0 \tag{35}$$

where $\Delta V_{CPD}$ is the relative voltage, $V_{CPD}$ is the absolute voltage, and $V_0$ is the initial reading of $V_{CPD}$ following charge deposition. Plotting voltages offset by the initial value gave a clearer comparison of $V_{SB}$ decay rates, without the added visual confusion of varying $V_0$ values.

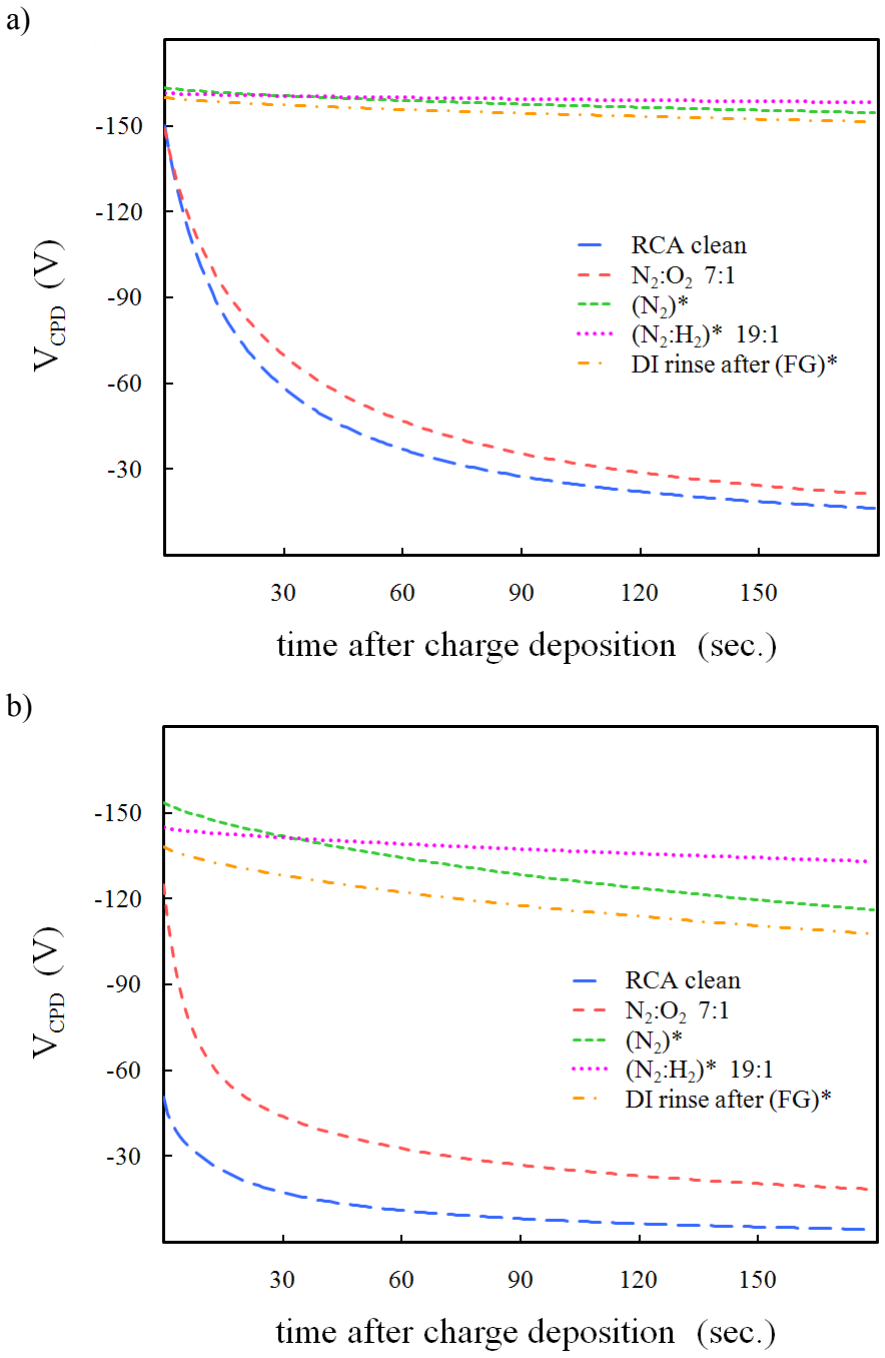


Figure 4.8. Depletion surface barrier decays obtained on n-type 4H-SiC epi-wafers A (a) and B (b) after various surface conditioning treatments, including ($N_2$:$H_2$)* or ($N_2$)* afterglow exposure and non-excited $N_2$:$O_2$ media at 600°C for 20 min., DI water rinsing after (FG)* conditioning, and standard RCA cleaning. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$.

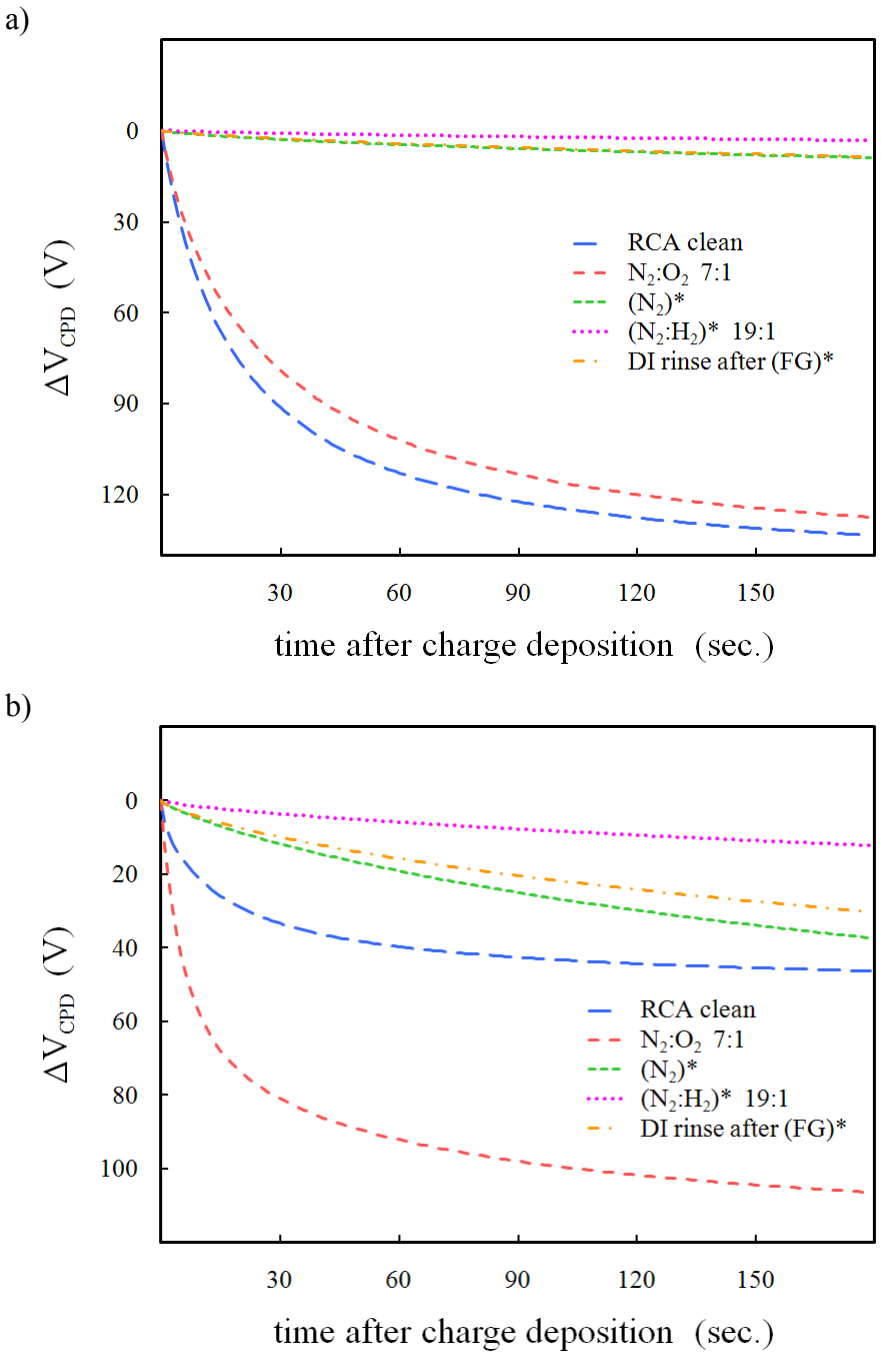


Figure 4.9. Depletion surface barrier transients obtained on n-type 4H-SiC epi-wafers A (a) and B (b) after various surface conditioning treatments, plotted relative to initial measured voltage to aid visualization of $V_{SB}$ decay rates. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Forming gas $(N_2{:}H_2)$* afterglow treated surfaces exhibited the slowest rates of $V_{SB}$ decay among all treatments including pure $(N_2)$* afterglow.

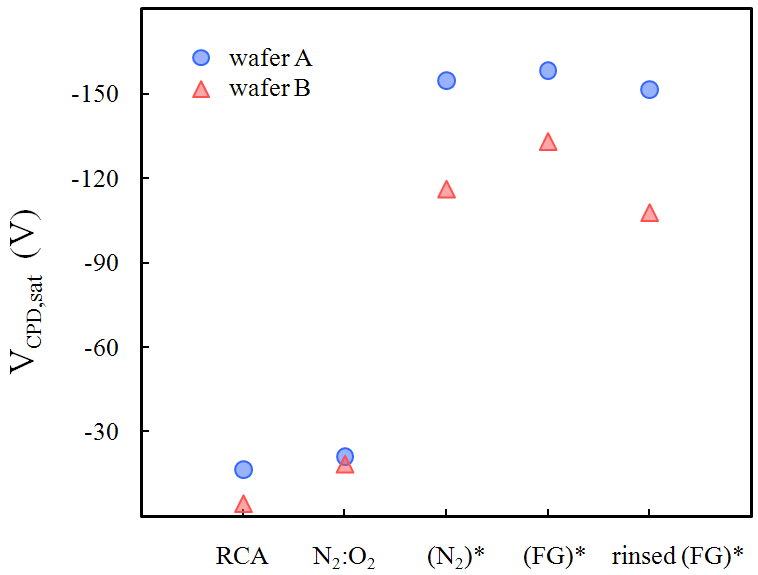


Figure 4.10. Final voltage values of depletion surface barrier transients obtained on n-type 4H-SiC epi-wafers after various surface conditioning treatments. Each $V_{sat}$ value is the wafer average of the final voltage value obtained after 3 minutes of decay. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Forming gas $(N_2:H_2)$* afterglow treated surfaces exhibited the highest $V_{sat}$ values among all treatments including pure $(N_2)$* afterglow.

Figure 4.10 contains the $V_{sat}$ values which corresponded to the average final voltage values obtained after 3 minutes of measurement. The $V_{sat}$ value in figure 4.10 was exactly the last voltage measured after 180 sec. of decay in figure 4.8. A higher value of $V_{sat}$ indicated less charge compensation and improved surface passivation.

An examination of the $V_{CPD}$ decays revealed that forming gas $(N_2:H_2)$* afterglow was the most effective at reducing concentrations of charge-emitting surface defects, indicated by the slowest decay rate and highest $V_{sat}$ of the treatment options. However, surface conditioning in pure $(N_2)$* afterglow at 600°C for 20 min. also achieved a very low rate of $V_{SB}$ decay, although the observed rate of 9V over 3 min. (wafer A) was not as slow as the 3V of decay obtained after (FG)* afterglow treatment. Evidenced by the electrical surface behavior, the 5% $H_2$ present in the FG mixture did have an impact on

cleaning and passivation of the semiconductor surface, perhaps due to contaminant removal and termination of dangling bonds and chemical surface states. Hence the combination of $N_2$ and $H_2$ afterglow was more effective at surface defect reduction and passivation than pure $N_2$ alone.

Following the standard (FG)* afterglow conditioning, rinsing of the surface in DI water did result in faster $V_{SB}$ decay rates relative to as-treated surfaces, although the difference in transient behavior was not large. In fact, (FG)*-conditioned surfaces after DI rinse still performed comparable or slightly better than the pure $(N_2)$* afterglow treatment. Based on this observation, one might suggest that DI rinsing removed the majority of the bond termination and defect passivation accomplished by the inclusion of $H_2$ in the afterglow media. Simply put, the water rinse possibly removed some hydrogen from the surface.

Exposing 4H-SiC surfaces to non-excited $N_2$:$O_2$ 7:1 at 600°C for 20 min. seemed to accomplish little more than the basic RCA clean. Depletion $V_{SB}$ decay rates were very fast and $V_{sat}$ values were low following $N_2$:$O_2$ treatment, implying that concentrations of surface defects for charge compensation were comparable to RCA cleaned surfaces. Thus the standard furnace temperature profile and exposure to nitrogen-containing ambient were not sufficient in and of themselves to produce any significant reduction of surface charge-emitting defects. The afterglow species of $N_2$ and $H_2$ microwave discharge were suggested as critical to the bond termination, defect passivation, and contaminant removal effects which resulted in the observed lowering of $V_{SB}$ decay rate.

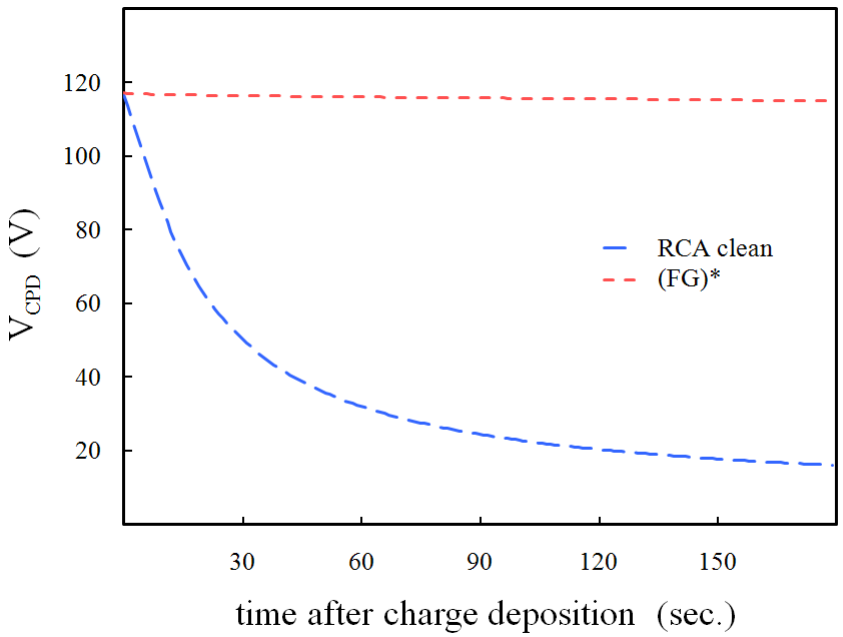


Figure 4.11. Depletion $V_{SB}$ transients obtained on p-type 4H-SiC 1 $cm^2$ sample comparing RCA clean to (FG)* afterglow surface conditioning for 20 min. at 600°C. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C $cm^{-2}$. (FG)*-treated p-type material demonstrated a much slower rate of $V_{SB}$ decay than RCA cleaned surfaces.

The majority of surface conditioning experiments for the purpose of $V_{CPD}$ transient evaluation in this work were investigated on n-type 4H-SiC material. For completeness, a small selection of experiments included p-type samples in order to confirm that the general trends of conditioning effects were not exclusive to n-doped material. Figure 4.11 gives an example of $V_{CPD}$ transient behavior on a 1 $cm^2$ p-type 4H-SiC sample, comparing the RCA cleaned surface to the standard $(N_2{:}H_2)$* afterglow treatment. A dose of $2.4\times10^{-7}$ C $cm^{-2}$ of positive corona ion density was used to pulse the p-type semiconductor into depletion, followed by $V_{SB}$ transient monitoring. Consistent with findings on n-type SiC, the RCA cleaned surfaces showed very fast decay rates, while the (FG)*-conditioned surfaces demonstrated extremely slow rates of $V_{SB}$ decay. In the case

of p- type material, the depletion surface potential barrier was positive. Both $V_{CPD}$ transients began around the same $V_0$ value of 117V. The surface barrier on RCA cleaned surfaces decreased very rapidly, with approximately 100V of decay during the 3 min. measurement, while the (FG)*-treated surface demonstrated only 2.3V of decay over the identical time interval. Thus on both p-type and n-type 4H-SiC semiconductors, (FG)* afterglow conditioning provided an effective means of surface passivation and reduction of charge-emitting defects, and produced the slowest rates of depletion $V_{SB}$ decay among the various treatments investigated.

### 4.3. $(N_2:H_2)$* afterglow treatment variations: time, temperature, durative stability

The use of forming gas $(N_2:H_2)$* afterglow was demonstrated to be a superior method of surface passivation and charge-emitting defect elimination. The slowest rates of $V_{SB}$ decay and highest $V_{sat}$ were achieved on (FG)*-conditioned 4H-SiC surfaces among other selected treatments including pure $(N_2)$* afterglow, non-excited media, and wet cleaning. Further investigation was required to reveal how the choice of treatment time and temperature impacted the proficiency of the (FG)* surface conditioning. For this purpose, an additional set of experiments incorporated variations of time and temperature to compare to the standard baseline parameters of 20 min. exposure at 600°C. Depletion $V_{CPD}$ transient decays were used to evaluate the effectiveness of each (FG)* treatment variation in passivating surface charge-emitting defects. Also, a separate set of experiments examined the stability of the (FG)*-treated surface in retaining its condition as a function of delay time and other post-treatment stresses.

Silicon carbide surfaces were conditioned for time intervals of 2.5−20 min. in (FG)* afterglow media at 600°C furnace temperature. All experimental conditions were

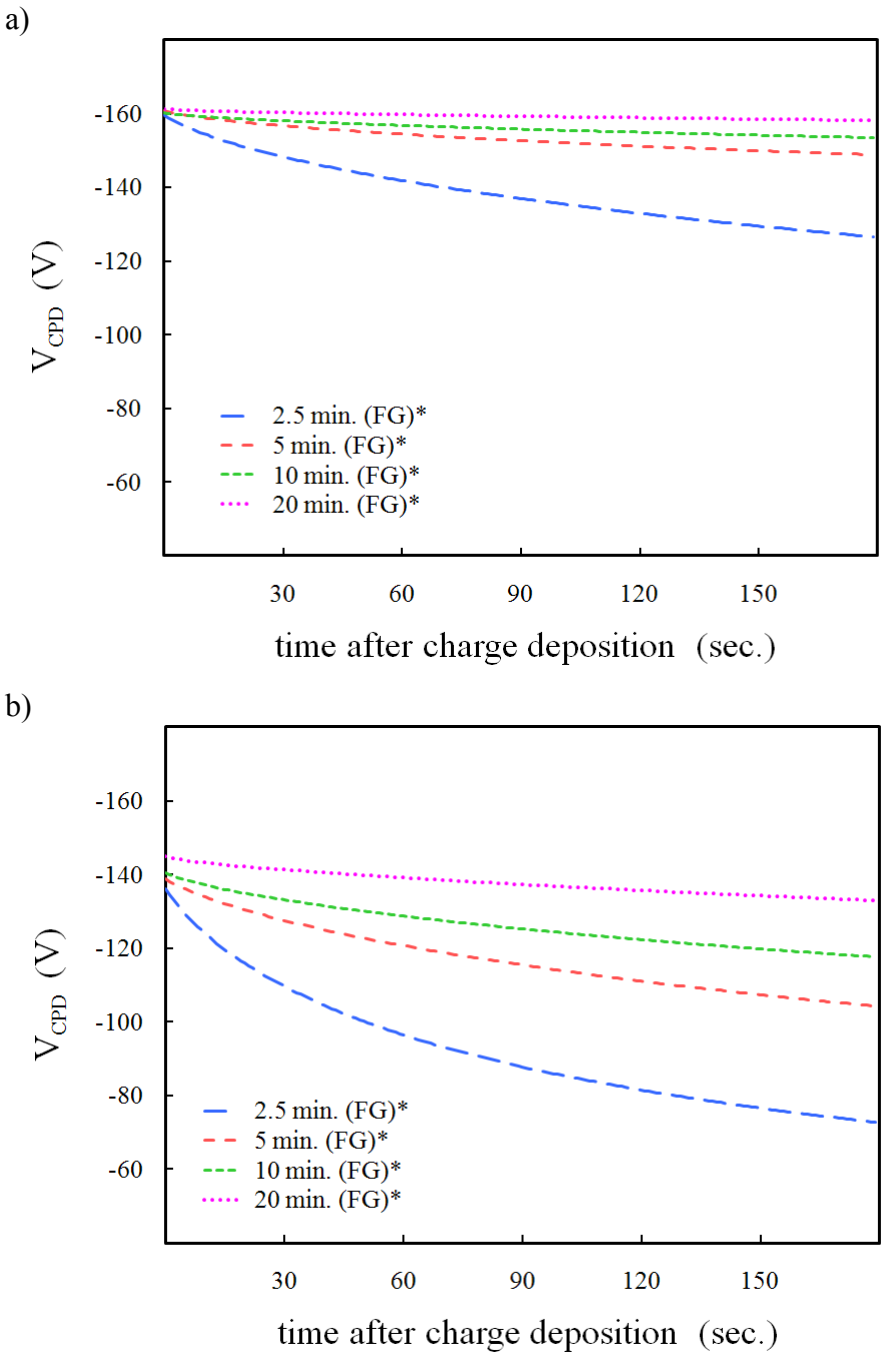


Figure 4.12. $V_{SB}$ transient decays obtained on n-type 4H-SiC epi-wafers A (a) and B (b) following (FG)* afterglow treatment for various time intervals at 600°C. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Slower rates of $V_{SB}$ decay were achieved after longer treatment times.

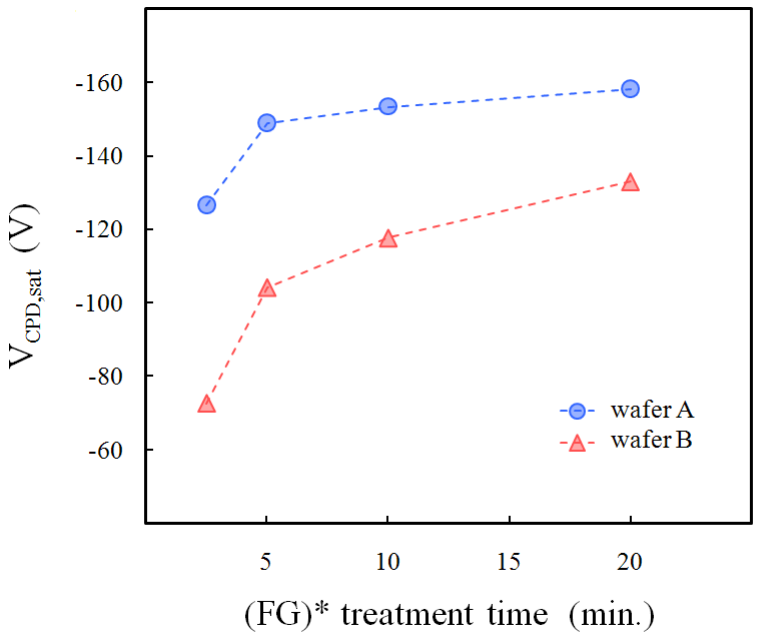


Figure 4.13. Final voltage values of depletion $V_{SB}$ transient decays obtained on n-type 4H-SiC epi-wafers following (FG)* afterglow treatment for various time intervals at 600°C. Each $V_{sat}$ value is the wafer average of the final voltage value obtained after 3 minutes of decay. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Higher $V_{sat}$ values and improved surface passivation were achieved after longer treatment time.

held constant except for the time of treatment. Investigation of depletion $V_{SB}$ transients revealed a distinct correlation between treatment time and resulting decay rate and uniformity. Initial $V_0$ values were similar, but the rate of $V_{CPD}$ decay increased as the treatment time was decreased, as seen in figures 4.12a and 4.12b for wafers A and B, respectively. The decays curves shown were averages of multiple wafer sites. The $V_{sat}$ values corresponding to the final voltages after 180 sec. of decay are shown in figure 4.13 as a function of treatment time. The largest concentration of surface charge-compensating defects was observed after the shortest treatment time of 2.5 min., resulting in an average 33V of decay on wafer A during the measurement interval ending with a $V_{sat}$ of −127V compared to only 3V of decay and $V_{sat}$ of −158V after the standard 20 min.

treatment time. Of the treatment durations studied, the longest treatment of 20 min. (FG)* afterglow provided the best surface passivation and charge-emitting defect reduction.

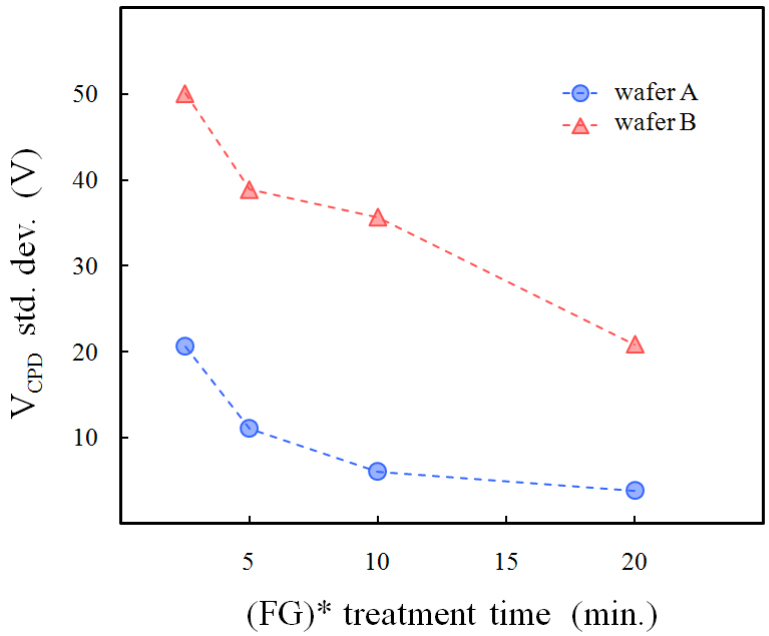


Figure 4.14. Uniformity of $V_{SB}$ transient decays obtained on n-type 4H-SiC following (FG)* afterglow treatment for various time intervals at 600°C. The standard deviation of $V_{CPD}$ was calculated from multiple wafer sites, and averaged over the 3 min. measurement interval. The deviation values shown were calculated from the data of the average $V_{CPD}$ decays in figure 4.12. The highest uniformity of surface condition was achieved at the longest treatment time of 20 min. (FG)* afterglow.

To examine the uniformity of the treated surface condition as a function of treatment time, the standard deviation of $V_{CPD}$ was calculated and averaged over the 3 min. measurement interval. Figure 4.14 contains the uniformity calculated values which displayed a trend of decreasing $V_{CPD}$ deviation with increasing (FG)* treatment time on both wafers A and B. Thus the longest treatment time of 20 min. (FG)* afterglow

resulted in the lowest deviation of depletion $V_{SB}$ decay behavior across the wafer and hence the highest uniformity of surface condition achieved during treatment.

Forming gas afterglow conditioning processes were performed at temperatures of 400°C−800°C to examine the dependence of surface passivation effects on thermal energy input. In each experiment, 4H-SiC wafers were RCA cleaned, loaded in the afterglow furnace under $N_2$ flow at 400°C, ramped up in non-excited $N_2$:$O_2$ 7:1 media to a specified treatment temperature (400−800°C), conditioned in ($N_2$:$H_2$)* 19:1 afterglow for the standard 20 min. interval, immediately unloaded under $N_2$ flow, cooled in cleanroom ambient, and characterized. Resulting $V_{CPD}$ transients after (FG)* conditioning of 4H-SiC surfaces at different temperatures are depicted in figures 4.15a and 4.15b for wafers A and B, respectively. Some temperature dependence was apparent in the rates of $V_{SB}$ decay. The $V_{CPD}$ curves were also plotted relative to $V_0$, to facilitate easier visualization of decay rates (figures 4.16a and 4.16b, wafers A and B, respectively). The final voltage values of the depletion $V_{CPD}$ decays are displayed in figure 4.17 as a function of treatment temperature.

Apparently, a thermal energy threshold existed between conditioning temperatures 500°C and 600°C. Forming gas (FG)* afterglow surface treatment performed at the low temperatures 400°C and 500°C resulted in much higher rates of $V_{SB}$ decay and lower $V_{sat}$ values, in fact an order of magnitude faster than decays obtained from treatment temperatures 600°C−800°C. Evidently, a temperature of at least 600°C was needed to provide the required thermal activation of surface passivation processes which occur during the ($N_2$:$H_2$)* afterglow conditioning of 4H-SiC. However, increasing the temperature to 700°C or 800°C produced quite similar depletion $V_{SB}$ transients compared

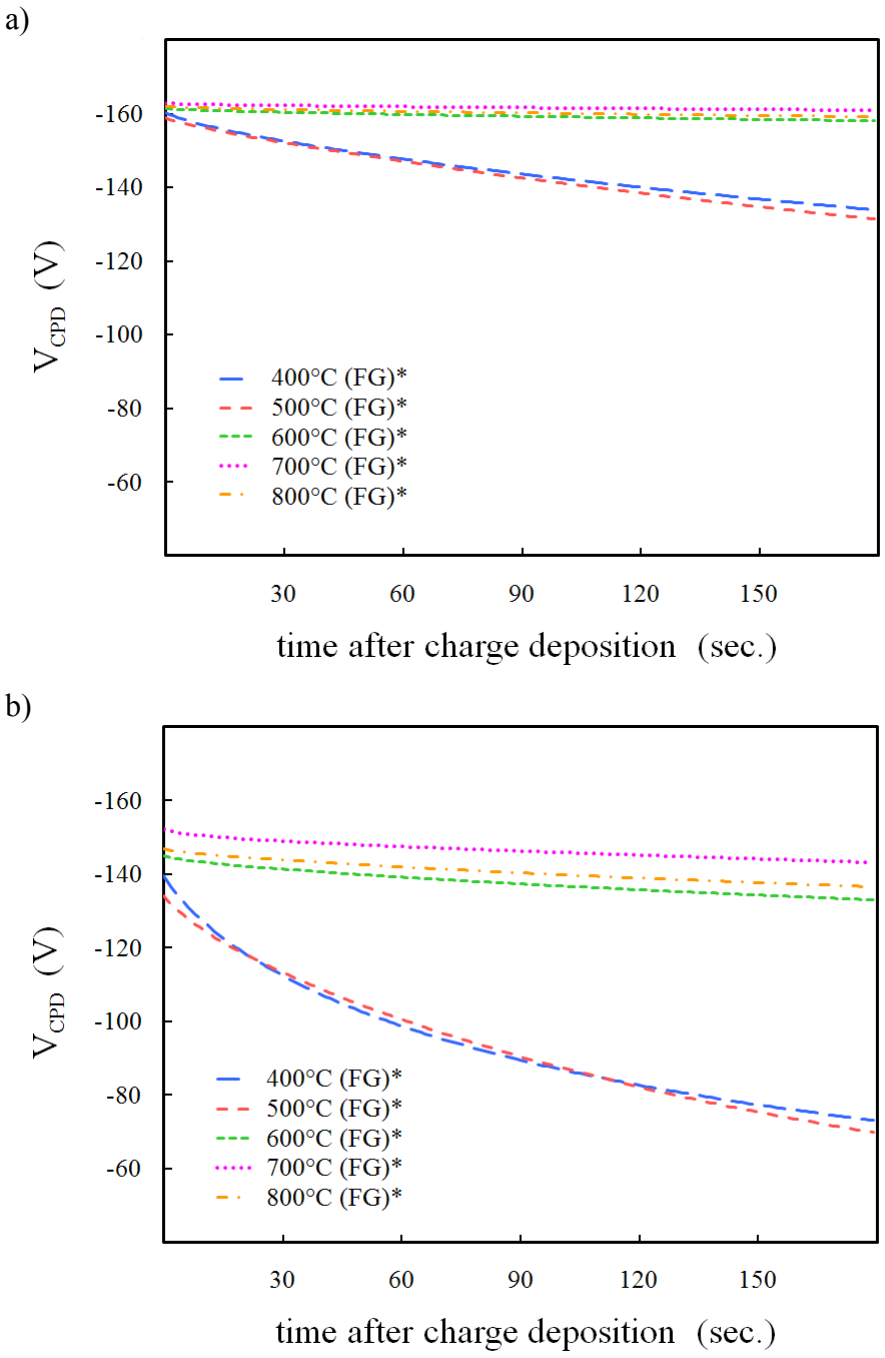


Figure 4.15. Depletion $V_{SB}$ transients obtained on n-type 4H-SiC epi-wafers A (a) and B (b) following (FG)* afterglow conditioning for 20 min. at treatment temperatures in the range 400°C−800°C. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$.

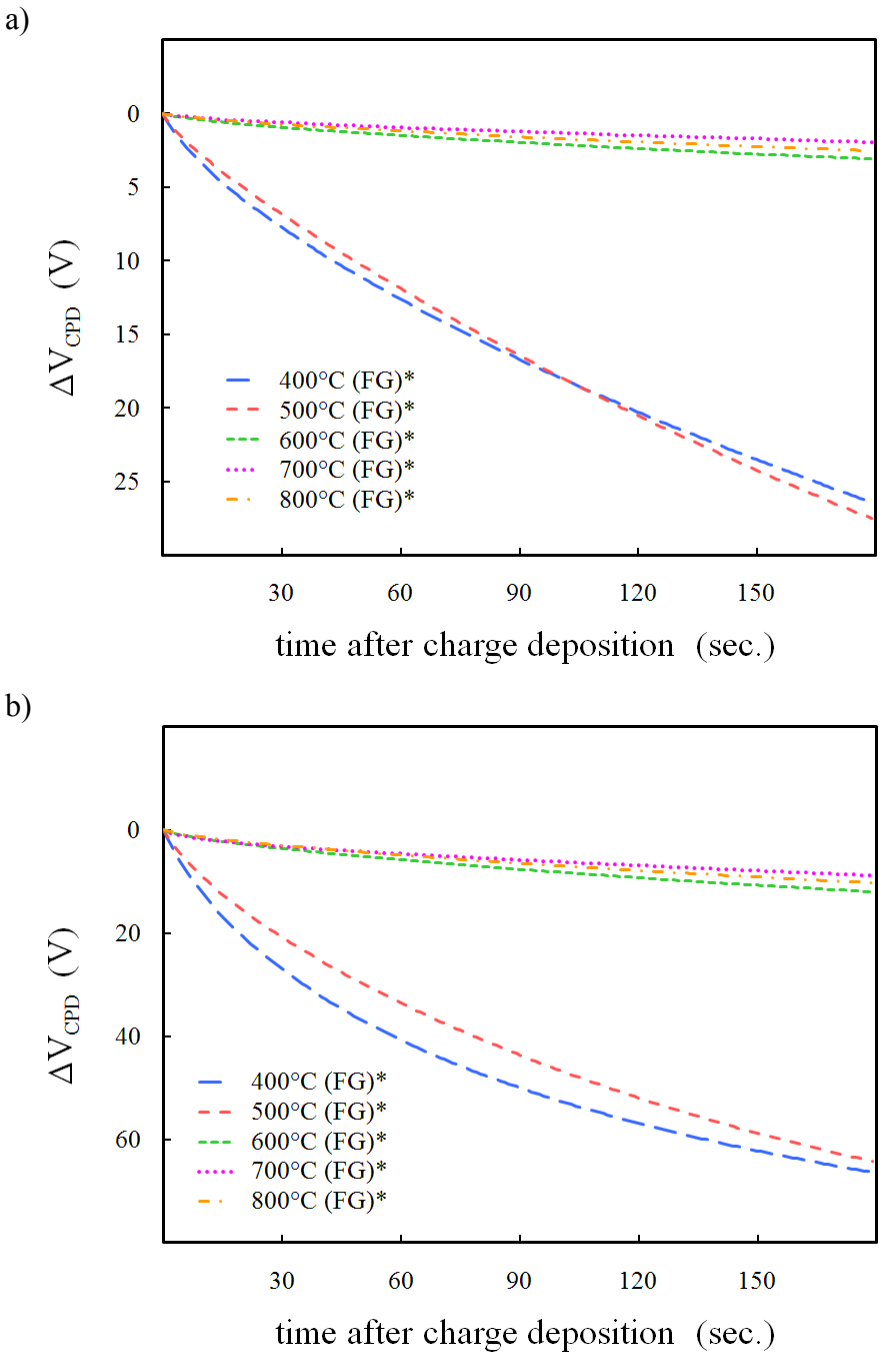


Figure 4.16. Depletion $V_{SB}$ transients obtained on n-type 4H-SiC epi-wafers A (a) and B (b) following (FG)* afterglow conditioning for 20 min. at various treatment temperatures, plotted relative to initial measured voltage to aid viewing of $V_{SB}$ decay rates. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Forming gas (FG)* conditioning at temperatures 600°C or higher resulted in an order of magnitude slower rate of $V_{SB}$ decay, indicating a thermal energy threshold exists between 500°C and 600°C (FG)* treatment temperature.

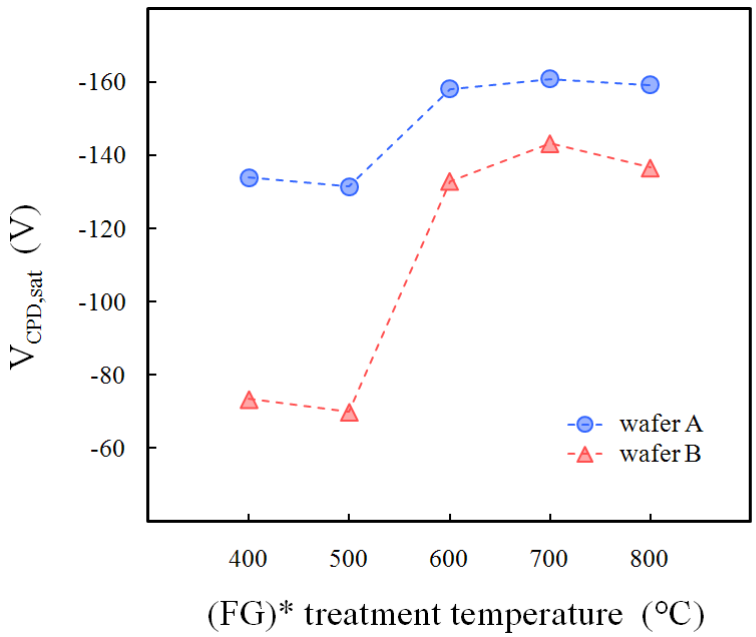


Figure 4.17. Final voltage values of depletion $V_{SB}$ transients obtained on n-type 4H-SiC epi-wafers following (FG)* afterglow conditioning for 20 min. at treatment temperatures in the range 400°C−800°C. Each $V_{sat}$ value is the wafer average of the final voltage value obtained after 3 minutes of decay. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C cm$^{-2}$. Forming gas (FG)* conditioning at temperatures 600°C−800°C resulted in higher $V_{sat}$ values compared to treatments at 400°C−500°C, indicating a thermal energy threshold exists between 500°C and 600°C (FG)* treatment temperature.

to 600°C. It should also be noted that prior work investigated the (FG)* conditioning of as-grown 4H-SiC epitaxial material at temperatures between 600°C−1100°C? [67]. Atomic force microscopy revealed a minimum in resulting surface roughness after (FG)* conditioning between 600–700°C. Judging from these results, 600–700°C is an optimal choice of (FG)* afterglow conditioning temperature in order to accomplish the combined effects of surface smoothing and defect passivation.

Most of the $V_{CPD}$ transient results presented in this work were obtained after minimal delay following surface treatment, in an effort to ensure that any change in surface condition over time would not impact the characterization results. However,

certain measurements were performed with the specific intent of testing the stability of surface condition to time delay after (FG)* afterglow treatment. $V_{CPD}$ transient decays were measured on consecutive days following a 20 min. (FG)* surface treatment at 800°C. $V_{SB}$ decays were obtained immediately after treatment, and at 24-hour intervals up to 3 days later. Following each measurement, wafers were exposed to light and stored in plastic Fluoroware cases until the next day. The surfaces were not rinsed in DI water or disturbed in any other way between measurements. The time-delayed $V_{CPD}$ decays are depicted in figures 4.18a and 4.18b for wafers A and B, respectively. Each curve shown is the average of multiple wafer sites. The observed rate of $V_{SB}$ decay was very consistent from day to day. The curve slope after the 3$^{rd}$ day of delay was practically identical to that obtained initially after the (FG)* surface treatment. The retention of $V_{SB}$ transient behavior over time provided strong evidence to support the suggestion that ($N_2$:$H_2$)* afterglow conditioning of 4H-SiC achieved a stable and resilient state of surface passivation.

Other aspects of surface condition stability in addition to time delay were investigated on n- and p-type 4H-SiC 1 cm$^2$ samples. $V_{CPD}$ transients were recorded immediately after the standard (FG)* afterglow treatment for 20 min. at 600°C. Following initial $V_{CPD}$ decay measurements, the surfaces were electrically stressed with a large corona pulse of opposite charge polarity, to achieve accumulation of majority carriers at the semiconductor surface and eliminate any space-charge remaining from the previous depletion voltage decay measurement. After accumulation stress and light exposure, the standard $V_{CPD}$ transient measurement was repeated with another depletion pulse of corona charge. Then the wafers were stored in plastic cases and measured again

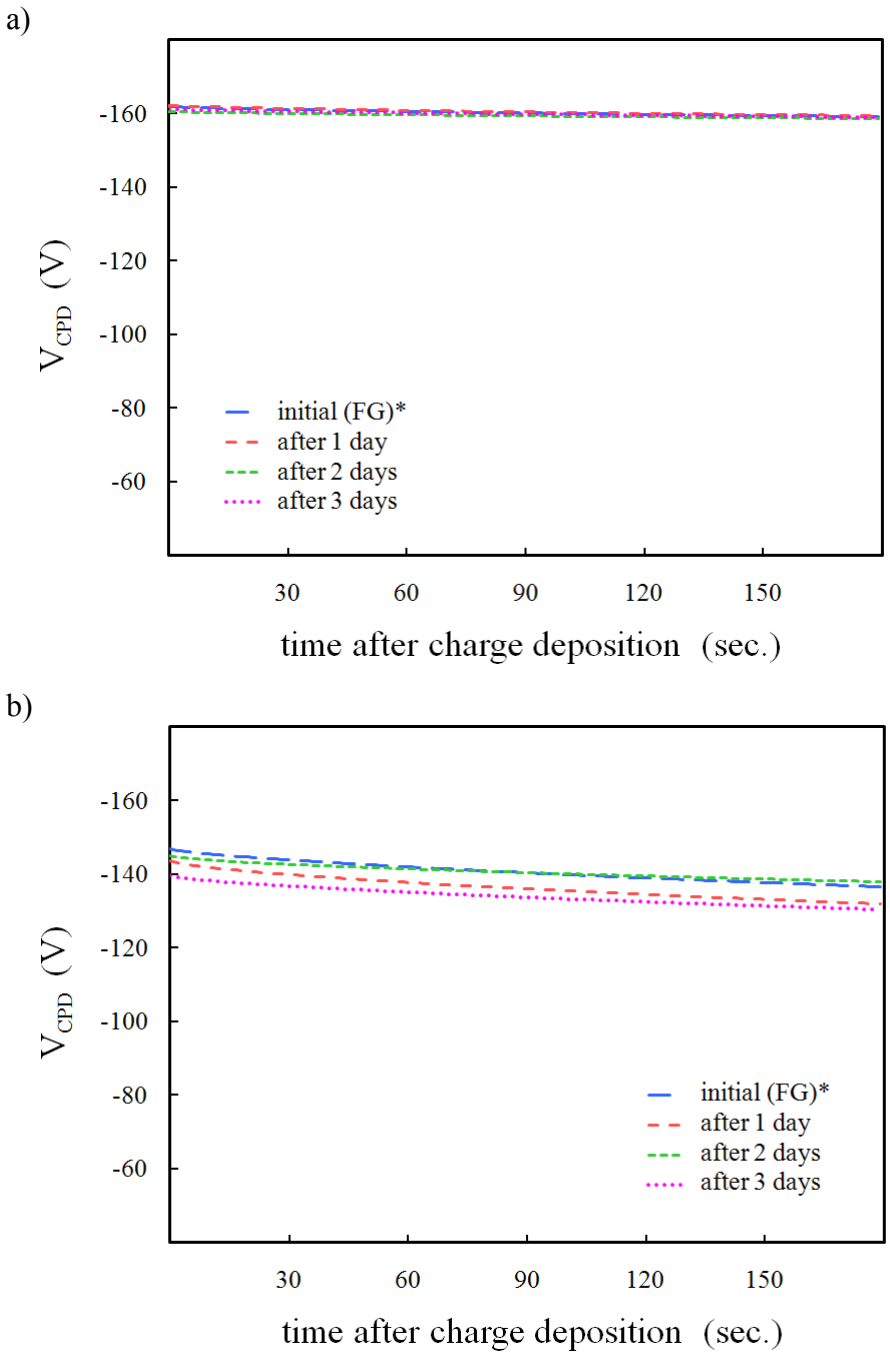


Figure 4.18. Depletion surface barrier decays obtained on n-type 4H-SiC epi-wafers A (a) and B (b) following (FG)* afterglow conditioning for 20 min. at 800°C, and remeasured after 1 day intervals of time delay. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C$ = $2.4\times10^{-7}$ C cm$^{-2}$. The resulting surface condition prepared by (FG)* afterglow treatment was quite stable, showing consistent rates of $V_{SB}$ decay many days after treatment.

after 6 days of storage. Following $V_{CPD}$ transient measurement on the 6th day, the samples were heated for 60 min. on a hotplate at 170°C in cleanroom ambient. After heating, depletion surface barrier decays were measured a final time. The resulting depletion $V_{SB}$ transient curves are shown in figures 4.19a and 4.19b for n- and p-type 4H-SiC, respectively. The condition of (FG)*-treated surfaces seemed to be very stable. All curves demonstrated similar starting voltages and rates of decay. No significant deviation in $V_{CPD}$ depletion response was caused by a combination of accumulation electrical stress, thermal stress, air exposure, or time delay. It was concluded that the improved state of defect termination and surface passivation suggested to exist after $(N_2{:}H_2)$* afterglow treatment of 4H-SiC demonstrated an enduring resilience and stability in retaining the surface conditioning effects while exposed to temporal, thermal, electrical, and environmental stresses.

$V_{CPD}$ transient metrology was used as a tool for electrical evaluation of 4H-SiC surfaces. The observed slow temporal decay of the depletion surface barrier was attributed to charge compensation through field-enhanced carrier emission from deep-level surface traps and recombination with space-charge dopant ions. Slower rates of $V_{SB}$ decay were suggested to be correlated with fewer charge-emitting surface defects. Surface conditioning treatments were examined to further investigate the effects of (FG)* afterglow exposure as a pre-oxidation surface preparation protocol. Of the various treatments, including wet cleaning, non-excited thermal treatment, and pure $(N_2)$* afterglow, the a superior effectiveness of charge-emitting defect reduction and surface passivation was achieved by forming gas $(N_2{:}H_2)$* afterglow exposure. A trend of decreasing decay rates and improvement in uniformity of surface condition was observed

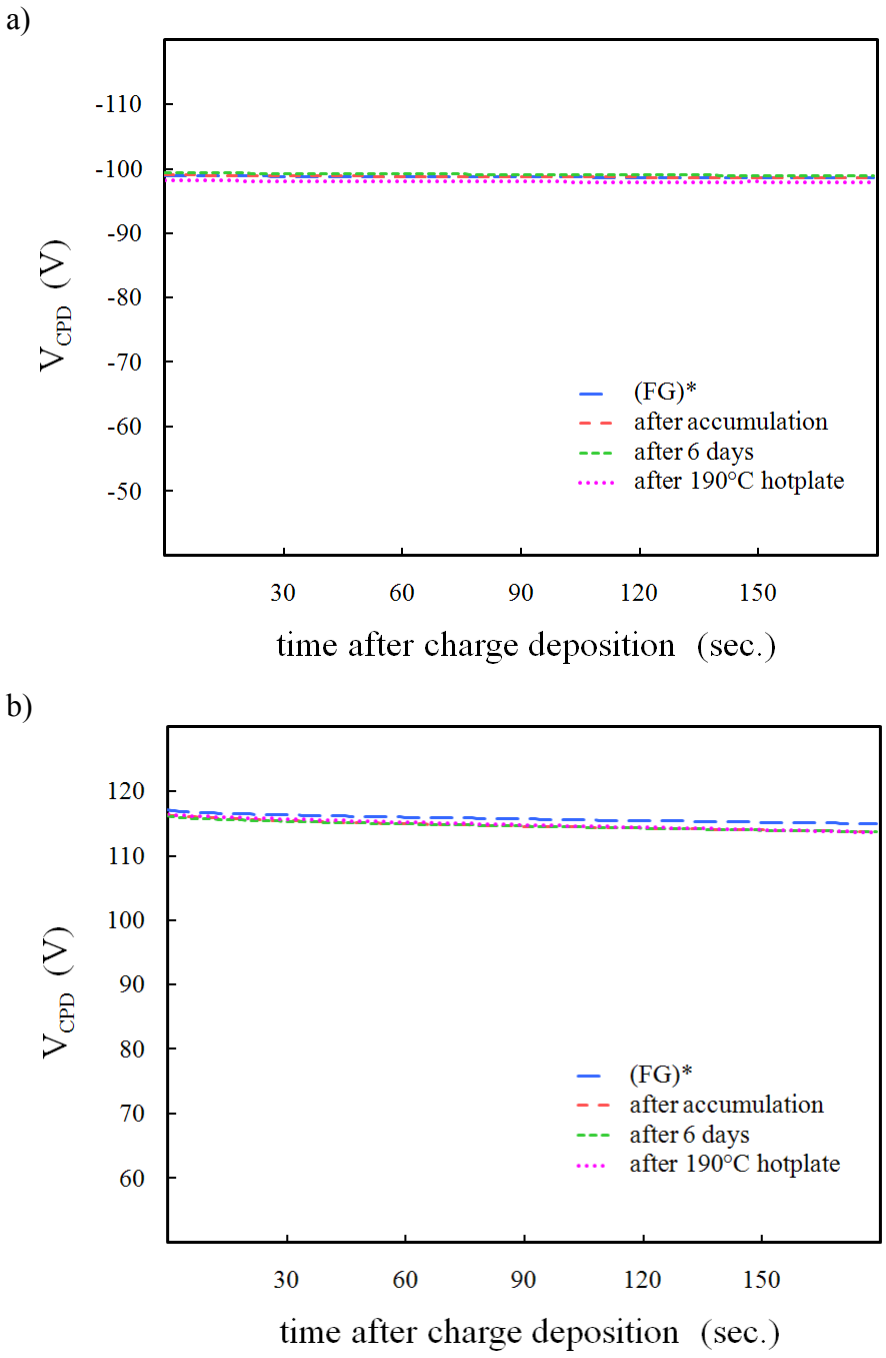


Figure 4.19. Depletion surface barrier decays obtained on n-type (a) and p-type (b) 4H-SiC 1 $cm^2$ samples following (FG)* afterglow conditioning for 20 min. at 600°C, and remeasured after accumulation corona stress, 6 day time delay, and heating in cleanroom ambient. Each curve is the average of multiple wafer sites. $V_{CPD}$ was monitored during 180 sec. following corona application of density $Q_C = 2.4\times10^{-7}$ C $cm^{-2}$. Observed rates of $V_{SB}$ decay remained stable even when the (FG)*-treated surfaces were exposed to temporal, electrical, thermal, and environmental stresses.

as treatment time was increased. A treatment temperature of 600°C or above was determined to provide the required thermal activation of the (FG)* afterglow conditioning process. The process parameters of 20 min. exposure at 600–700°C were identified as sufficient for a standard baseline (FG)* afterglow surface treatment of 4H-SiC. The resulting state of surface passivation was determined to be quite stable. Conditioning effects as observed by $V_{CPD}$ transient metrology were retained over significant periods of time following treatment, and were stable even when surfaces were exposed to various electrical, thermal and environmental stresses. The action of hydrogen and nitrogen afterglow species were suggested to be responsible for preparation of the SiC surface, with a combination of dangling bond termination, cleaning of contaminants, reduction of surface states, nitridation or nitrogen incorporation, Si-enrichment, and passivation or removal of C clusters and other C-related defects. The supplemental XPS metrology results of chapter 5 provided crucial chemical information to facilitate the continuation of an in depth analysis of the $(N_2{:}H_2)$* afterglow conditioning impact on 4H-SiC surfaces.

# Chapter 5. X-ray Photoelectron Spectroscopy of Conditioned 4H-SiC Surfaces

Chemical and elemental analysis and identification of SiC surfaces were crucial to the investigation of afterglow conditioning effects and the impact of such surface treatments on subsequent oxidation processing. Results of non-contact corona-Kelvin capacitance metrology revealed an increase in oxidation growth rate and improvement in film uniformity after preparing 4H-SiC surfaces by $(N_2{:}H_2)$* afterglow prior to oxidation. As indicated by C-KM $V_{CPD}$ transient decay measurements, (FG)* afterglow conditioning resulted in the lowest densities of charge-emitting surface defects among the other surface treatments considered. In addition to the primary metrology method of non-contact C-KM electrical measurements on semiconductor surfaces and oxide films, this work also incorporated XPS examination of 4H-SiC to determine the impact of (FG)* afterglow treatment on surface chemistry.

## 5.1. XPS measurement technique

The X-ray photoelectron spectroscopy technique essentially adapts a high-energy version of the photoelectric effect to identify binding energies of chemical species at the sample surface. High-energy photons (1−2 keV) impinge upon the sample surface from a monochromatic X-ray source. As the primary X-rays interact with core-level electrons, it is possible for any electron to be ejected if it has a binding energy $E_B$ less than the incident photon energy hν. Only electrons originating from the top 5−50 Å surface region are ejected from the sample, limited by the electron escape depth [68]. The

emitted photoelectrons arrive at the spectrometer with energy $E_{sp}$, where they are analyzed and counted. The electron energy at the analyzer will be related to the binding energy and the primary photon energy as follows:

$$E_B = h\nu - E_{sp} - q\Phi_{sp} \quad (36)$$

where $E_B$ is the core electron binding energy referenced to the Fermi energy $E_F$, hν is the primary X-ray energy, $E_{sp}$ is the energy of the ejected photoelectron arriving at the spectrometer, and $\Phi_{sp}$ is the spectrometer work function. The resulting XPS signal contains electron counts per second as a function of binding energy. Since the binding energy of an electron is influenced by its chemical state, XPS spectra allow determination of chemical compounds and elements in the sample surface. Software analysis of peak heights and widths with appropriate correction factors allows density calculations such as atomic percent of various elements. A measurement schematic and illustration of the electronic processes involved in XPS metrology are depicted in figures 5.1 and 5.2.

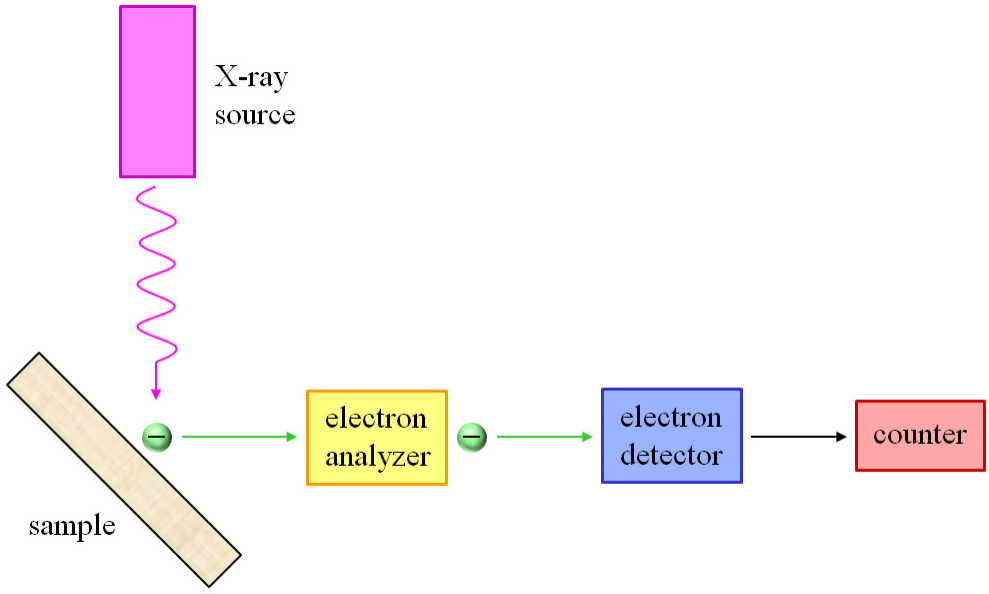


Figure 5.1. XPS measurement schematic.

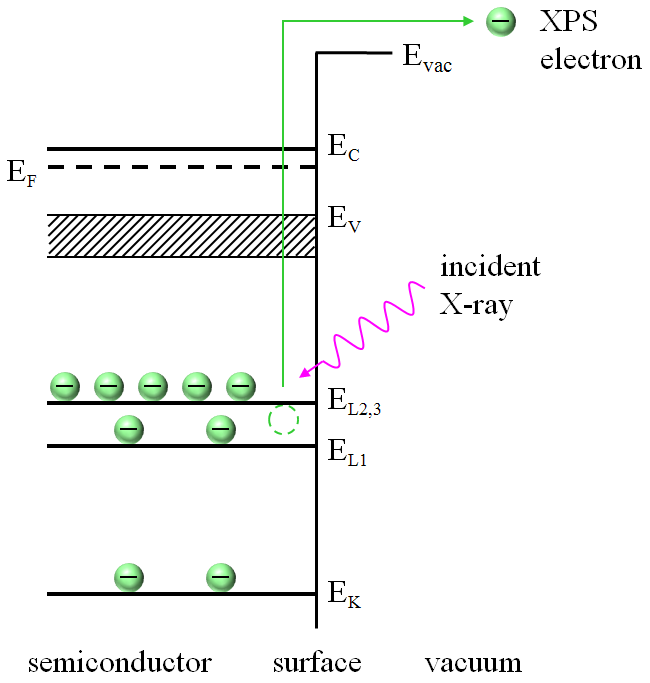


Figure 5.2. Electron energy band diagram illustrating photoemission of core level electrons in the XPS technique.

## 5.2. XPS results on 4H-SiC surfaces

XPS measurements were used to compare SiC surfaces prepared by (FG)* afterglow conditioning and RCA wet cleaning. XPS measurement service was provided by the lab of Fred Stevie at NCSU. XPS spectral data were analyzed using CasaXPS processing software [69]. After standard RCA cleaning of n-type 4H-SiC 1 $cm^2$ samples, some surfaces were conditioned by the baseline (FG)* afterglow process for 20 min. at 600°C. Afterglow conditioned samples were unloaded from the furnace at 600°C, allowed to cool in cleanroom ambient, and immediately shipped along with the RCA cleaned samples in Fluoroware cases for next-day measurement. XPS spectra were obtained on as-received surfaces, and after 2 min. sputtering with 5 keV $Ar^+$ source estimated to remove 4 Å of material.

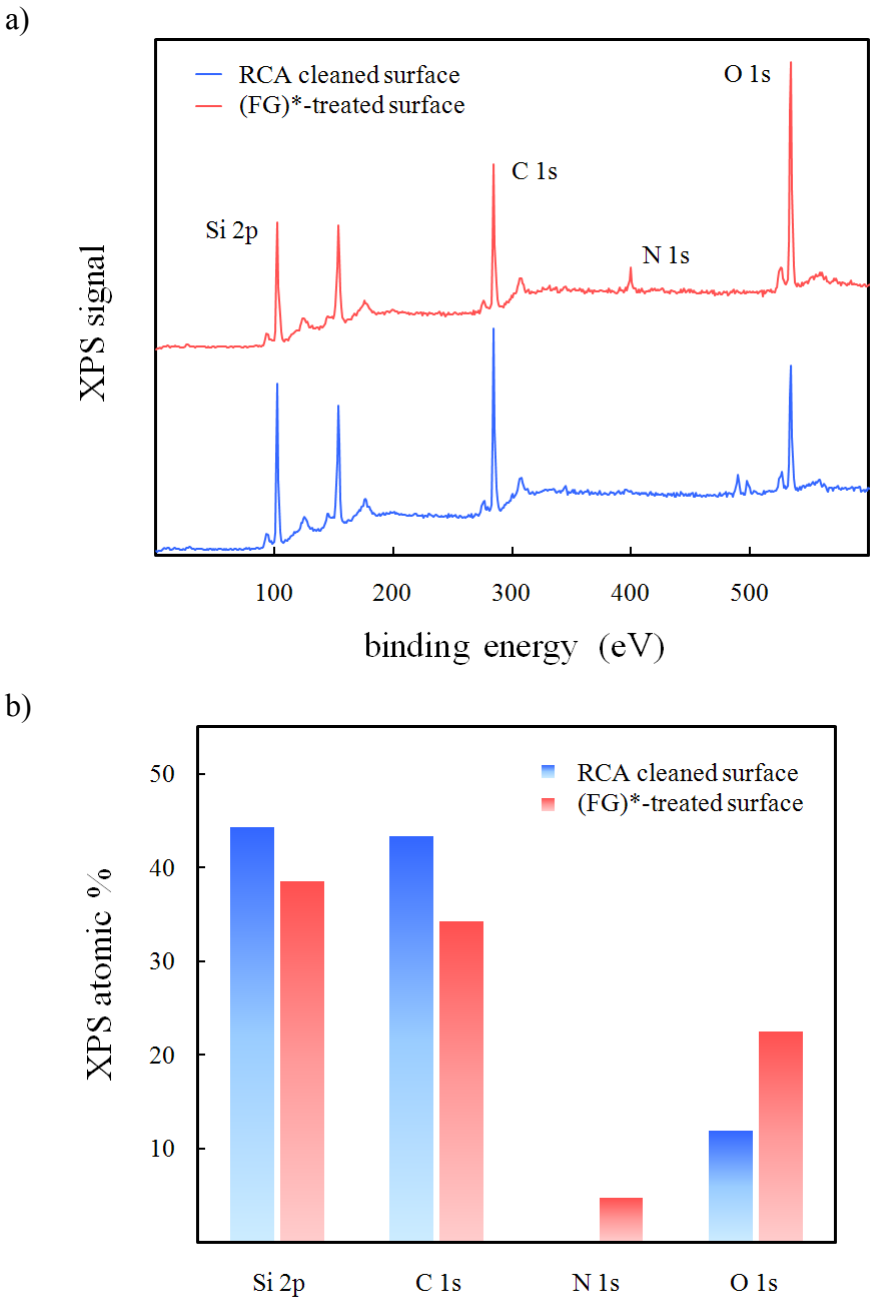


Figure 5.3. XPS spectral data (a) and atomic percent values (b) obtained on n-type 4H-SiC surfaces after RCA clean or (FG)* afterglow treatment.

Figure 5.3a compares the survey spectral data of the XPS signal obtained on 4H-SiC surfaces after RCA clean and (FG)* afterglow treatment. The XPS spectra shown in the figure were obtained on as-received surfaces after sample shipment, without any additional cleaning or sputtering. Atomic percent values of the elements of interest were calculated in CasaXPS and are displayed in figure 5.3b. Peaks around binding energies 102, 285, 400, and 534 eV were prominent in the XPS spectra, corresponding to the Si 2p, C 1s, N 1s, and O 1s core levels, respectively. Unfortunately, hydrogen was undetectable due to limitations of the XPS technique. All peaks obtained were single component signatures, absent of any evidence of superposition of neighboring peaks with closely spaced energies. Since the XPS technique is extremely surface sensitive [68], the results were used to identify chemical species in the first few monolayers of material.

The N 1s peak was only visible on the (FG)*-treated surface, and absent on the RCA cleaned surface. The presence of a small N 1s peak in the treated surface XPS spectra provided evidence of nitrogen incorporation during the (FG)* afterglow conditioning of 4H-SiC. The O 1s peak showed a relatively higher intensity on the (FG)*-conditioned surface compared to the RCA cleaned surface. The presence of oxygen on the RCA cleaned surface was primarily a result of native oxide formation and oxygen adsorption after the wet chemical cleaning procedure and during shipping. The larger percentage of oxygen observed on the (FG)*-treated surface was suggested to be a direct result of the afterglow processing unloading procedure. Following (FG)*-treatment, heated samples were unloaded from the furnace and allowed to cool in cleanroom air. The 600°C furnace unloading temperature was far below the previously mentioned threshold of 950°C required for thermal oxidation of SiC. Nonetheless, the

exposure of hot substrates to the oxygen content in air supports an increased amount of oxygen adsorption at the surface. Percentages of both C 1s and Si 2p after the (FG)* treatment were less than the RCA clean, primarily due to the increase in both oxygen and nitrogen content observed on the treated surface. Since the total percentage of all species was by definition 100, an increase of the O and N peaks required a decrease in percentages of other species (C and Si) on the (FG)*-treated surface. Additional significance was placed on the changes in ratios of species rather than absolute atomic percentages. The C/Si ratio was 0.978 on the RCA cleaned surface, and decreased to 0.891 on the surface conditioned in (FG)* afterglow. The reduction of C/Si ratio gave strong evidence in support of the removal of carbon from the SiC surface layers during (FG)* afterglow exposure. Carbon removal could contribute to the formation of a Si-rich surface region, but also could be part of the nitridation process responsible for the observed nitrogen incorporation at the surface. Thus the XPS spectra were consistent with a surface chemistry enriched in both Si and N achieved during afterglow conditioning.

Following XPS measurement of as-received surfaces, the samples were sputtered and remeasured. Sputtering for 2 min. with a 5 keV $Ar^+$ source was estimated to remove roughly 4 Å of material, on the order of one monolayer. Figure 5.4 contains an XPS comparison of the (FG)*-treated SiC surface before and after sputtering. The significant changes in XPS spectra caused by sputtering were a decrease of both nitrogen and oxygen percents, and a corresponding increase in Si and C content. Nitrogen atomic percent was reduced from 4.74 to 1.51 after sputtering. The presence of the N 1s peak even after sputtering implied some degree of nitridation and incorporation of N below the

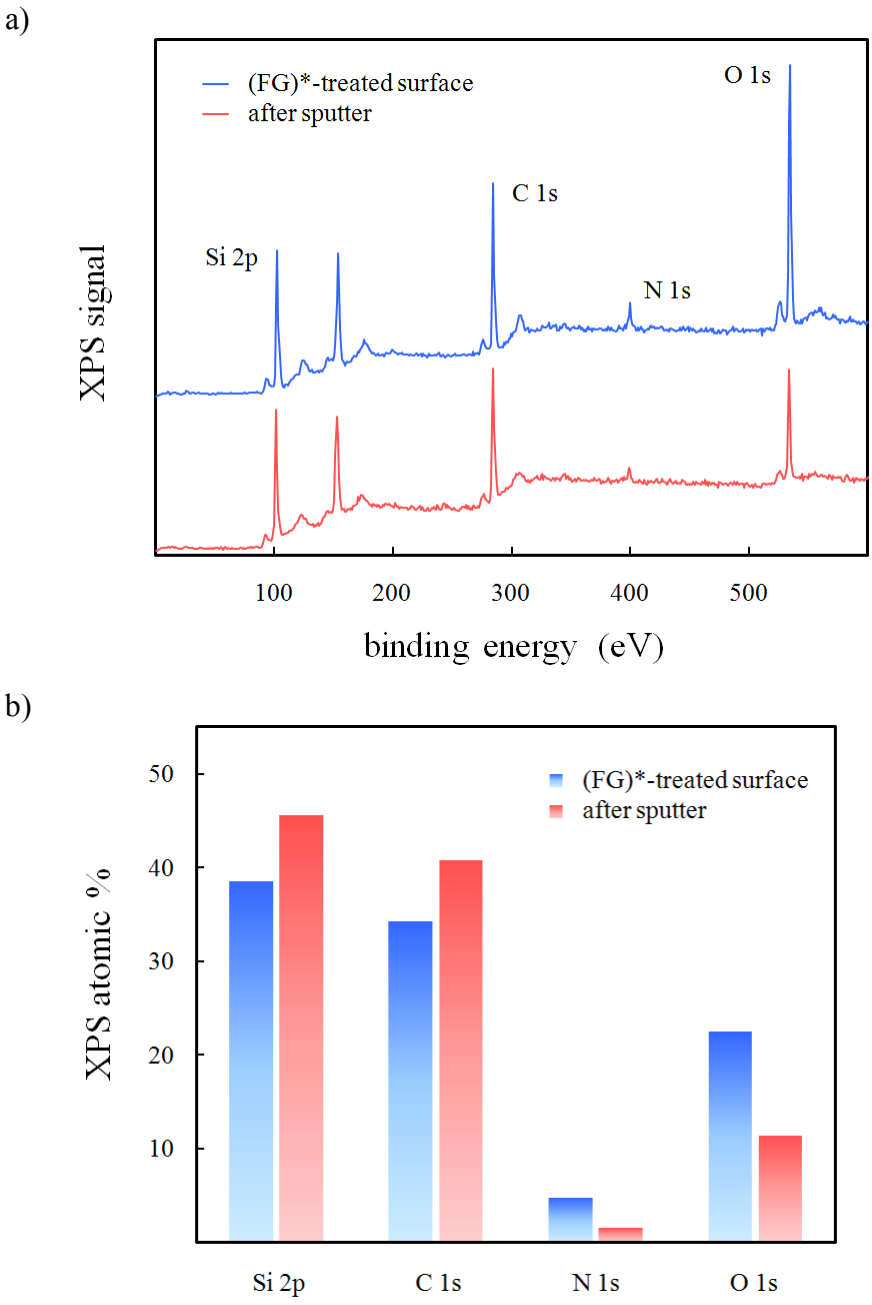


Figure 5.4. XPS spectral data (a) and atomic percent values (b) obtained on n-type 4H-SiC surfaces as treated by (FG)* afterglow, and after sputtering. Sputtering for 2 min. with 5 keV $Ar^+$ source was estimated to remove 4 Å of material from the sample surface.

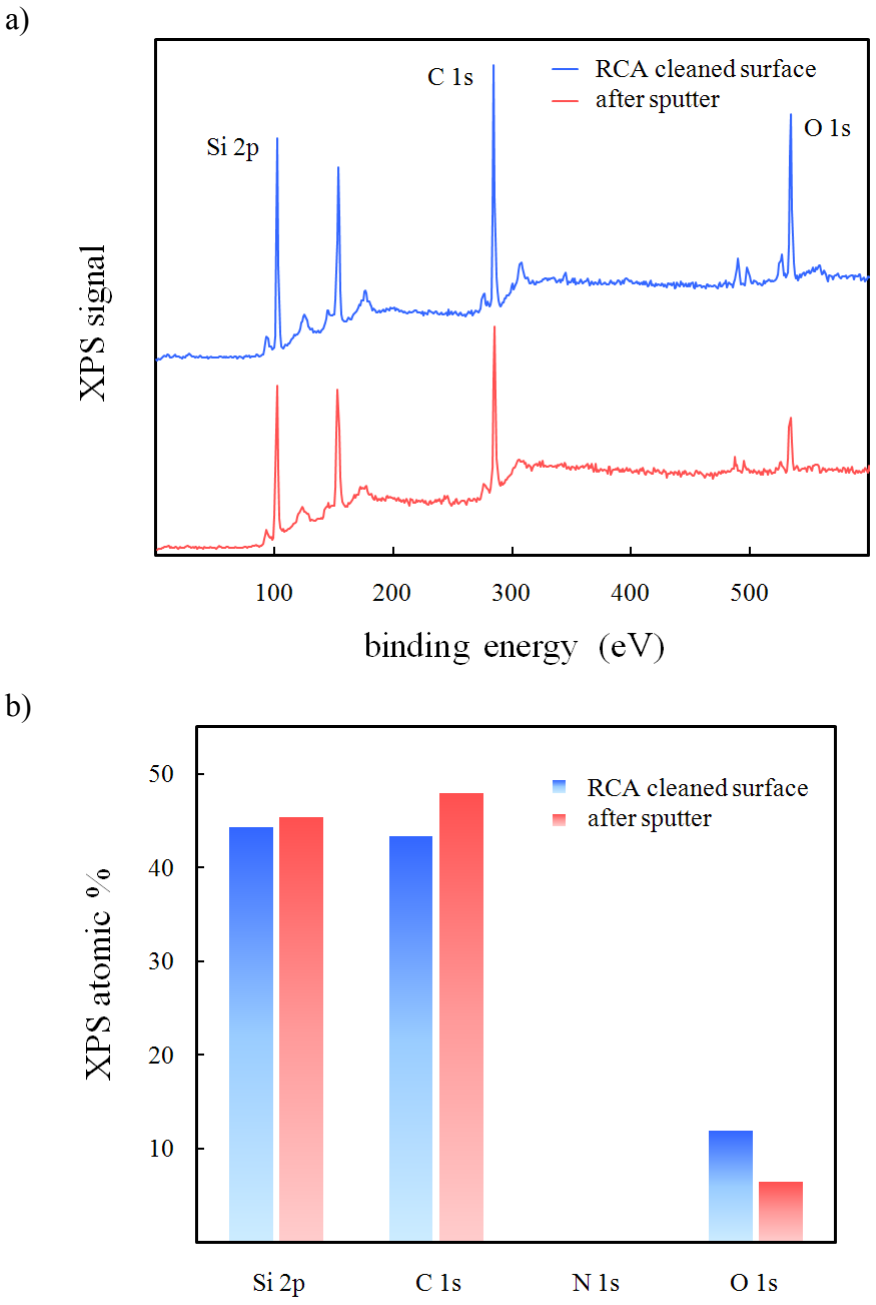


Figure 5.5. XPS spectral data (a) and atomic percent values (b) obtained on n-type 4H-SiC surfaces as treated by RCA clean, and after sputtering. Sputtering for 2 min. with 5 keV $Ar^+$ source was estimated to remove 4 Å of material from the sample surface.

topmost monolayer(s) during (FG)* treatment. The N 1s peak could not be dismissed as simply adventitious contamination. Both C and Si percentages increased after sputtering, as required by the aforementioned decreases in nitrogen and oxygen content. However, the C/Si ratio remained almost unchanged at 0.894, compared to 0.891 before sputtering. Even after material removal by sputtering, the relative carbon content remained lower, suggesting that the (FG)* afterglow effectively removed carbon at least from the top several monolayers.

Figure 5.5 displays the XPS data obtained before and after sputtering of the RCA cleaned 4H-SiC surface. Again, the N 1s peak was not present on the RCA cleaned surface. The O 1s peak was reduced after sputtering, with corresponding slight increases in both Si and C atomic percents. In this case, the C percentage increased more than the Si, yielding an increase in the C/Si ratio from 0.978 to 1.057 after sputtering. This was partially attributed to removal of roughly a monolayer of native oxide during sputtering, thus decreasing the relative Si (and O) content in the surface layers.

Figure 5.6 shows a comparison between the RCA clean and (FG)* afterglow treated surfaces, both after sputtering. In fact, the XPS differences were generally similar to the comparison of the surfaces before sputtering (figure 5.3). A small N 1s peak was visible on the (FG)*-treated sample after sputtering, which was not present on the RCA cleaned sample. The oxygen percentage was also higher for the (FG)* conditioning than the RCA clean. However, the Si percent on the (FG)*-treated sample was essentially identical to the RCA clean. This required a reduction in carbon percent to offset the small increases in nitrogen and oxygen content on the (FG)*-treated sample. As a result,

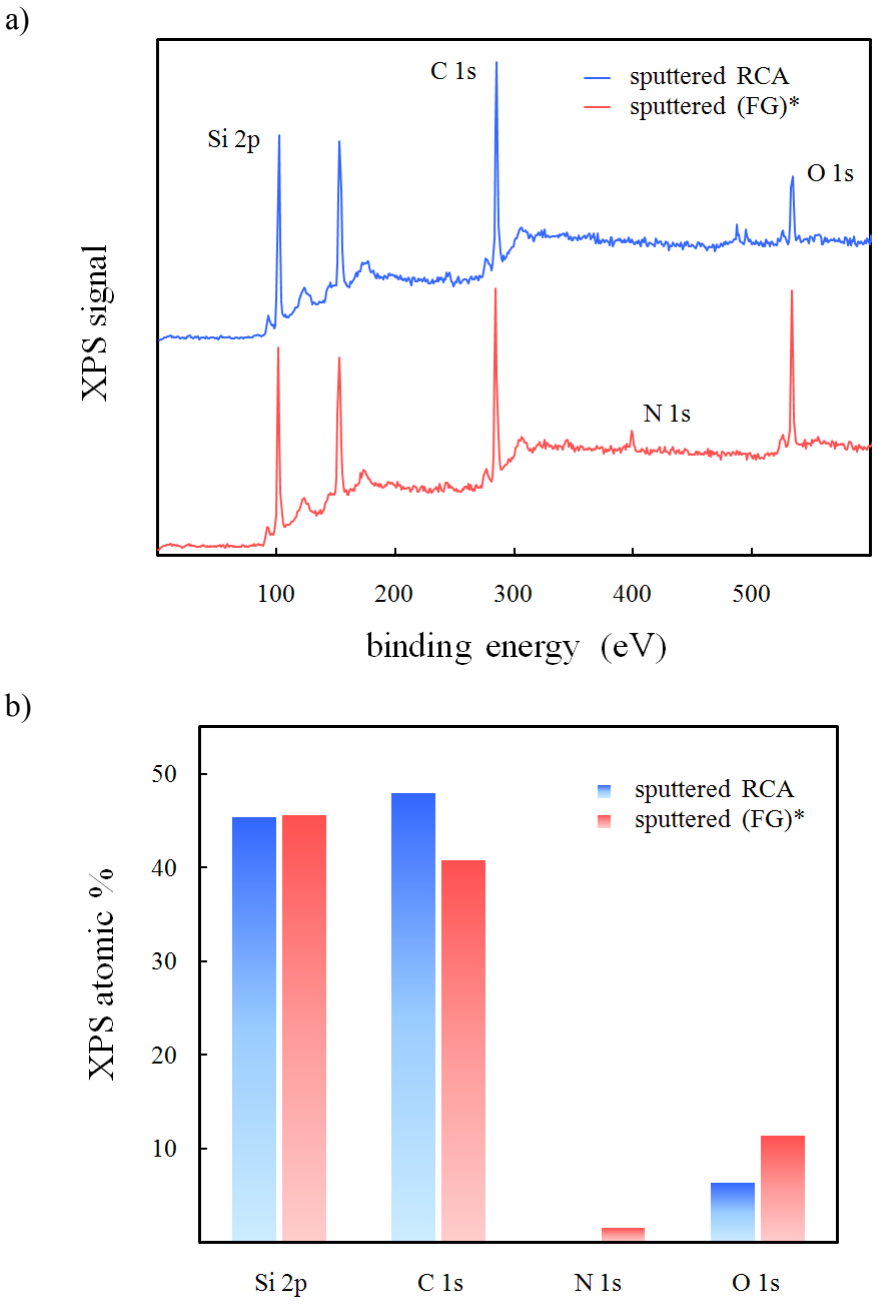


Figure 5.6. XPS spectral data (a) and atomic percent values (b) obtained after sputtering of n-type 4H-SiC surfaces treated by RCA clean or (FG)* afterglow. Sputtering for 2 min. with 5 keV $Ar^+$ source was estimated to remove 4 Å of material from the sample surface.

the C/Si ratio was significantly higher for the RCA clean (C/Si = 1.057) compared to the afterglow treatment (C/Si = 0.894). Thus, after sputtering removal of ~4 Å of material, the (FG)* afterglow treated sample still demonstrated strong indications of Si-enriched surface chemistry and some degree of nitrogen incorporation which were not evident on the RCA cleaned sample after sputtering. All atomic percentage values and ratios calculated by XPS analysis are summarized in table 5.1.

Table 5.1. XPS atomic percent and ratios of selected elements obtained on n-type 4H-SiC surfaces treated by RCA clean or (FG)* afterglow conditioning, before and after sputtering. Sputtering for 2 min. with 5 keV $Ar^+$ source was estimated to remove 4 Å of material from the sample surface.

| XPS atomic % | RCA clean | | (FG)* afterglow | |
|---|---|---|---|---|
| | surface | sputtered | surface | sputtered |
| Si 2p | 44.33 | 45.39 | 38.50 | 45.61 |
| C 1s | 43.37 | 47.96 | 34.29 | 40.78 |
| N 1s | — | — | 4.74 | 1.51 |
| O 1s | 11.90 | 6.41 | 22.47 | 11.34 |
| C / Si | 0.978 | 1.057 | 0.891 | 0.894 |
| O / Si | 0.268 | 0.141 | 0.584 | 0.249 |

The observed effects of (FG)* treatment on surface chemistry were consistent with the results of chapter 3 demonstrating the impact of surface conditioning on subsequent oxide film formation. An oxide film thickness increase of 10–20% was observed when the 4H-SiC surfaces were conditioned via (FG)* afterglow prior to oxidation. This increase in growth rate corresponded to approximately 2–25 additional monolayers of oxide film growth (~3.3 Å/layer), depending on growth time and temperature. The

preparation of a Si-rich surface region by afterglow conditioning, at least through the first several monolayers, might have contributed to additional oxide growth considering that the presence of carbon inhibits the oxidation process on SiC due to the higher C-Si bond energy. The removal of carbon and incorporation of nitrogen were also consistent with depletion surface barrier decay measurements presented in chapter 4. Afterglow surface conditioning was effective at reducing the rate of $V_{SB}$ decay, a result which was attributed to a reduction in the amount of charge emission from various surface defects. The XPS spectra obtained on (FG)*-conditioned surfaces suggested the elimination and passivation of C-related defects in the surface region as a contributing factor in the reduction of surface charge-emitting defect concentrations.

# Chapter 6. Conclusion

## 6.1. Results summary

Surface conditioning and oxidation of the wide band-gap semiconductor 4H-SiC were investigated using a novel sequential afterglow processing approach combined with the unique capabilities of non-contact corona-Kelvin metrology. The use of remote plasma assisted thermal oxidation facilitated film growth at low temperature and pressure with the flexibility of sequential *in-situ* processing options including pre-oxidation surface conditioning. Corona-Kelvin metrology provided a fast, non-destructive method for electrical evaluation of oxide films and semiconductor surfaces. Treatment in forming gas ($N_2$:$H_2$)* 19:1 afterglow was used to condition the SiC surface prior to remote plasma oxidation by ($O_2$:$N_2O$:$N_2$:$H_2$)* chemistry. The pre-oxidation (FG)* afterglow treatment step was found to have a significant impact on resulting oxide film thickness and thickness uniformity as determined by non-contact C-KM oxide capacitance-voltage measurements (chapter 3). Direct measurement of SiC surfaces for various treatment conditions was accomplished using non-contact C-KM depletion surface barrier decay monitoring (chapter 4) and XPS analysis of surface chemistry (chapter 5). Results were interpreted relating the impact of afterglow conditioning on the surface and its influence on subsequent oxide thin film growth as part of a sequential afterglow oxidation approach to the promising SiC material.

The results of oxide film characterization were presented in chapter 3 for afterglow oxides grown at various temperatures (600–850°C) and time intervals (10–90 min.). Prior to oxidation, an optional surface conditioning step exposed the 4H-SiC samples to (FG)* afterglow media for 20 min. at 600°C. Oxide thickness (EOT) values were extracted from C-KM capacitance characteristics. Preparation of the surface in (FG)* afterglow was found to produce an oxide growth rate increase (10-20% thicker films) and an improvement in oxide uniformity. The growth rate and uniformity improvements were more prominent at higher oxide growth temperatures. Based on the surface measurement findings of chapters 4 and 5, past experimental results, and supplemental information from the literature, the (FG)* afterglow conditioning of 4H-SiC was suggested to accomplish a combination of passivation of surface states and defects, removal of carbon and elimination of C-related defects, Si-enrichment of the surface layers, cleaning and removal of surface contaminants, nitrogen incorporation, and reduction of surface roughness. These conditioning effects were among the factors contributing to the observed impact on subsequent oxide formation. The removal of carbon during surface conditioning was particularly expected to enhance the oxide growth rate. Surface defect passivation, contaminant removal, and smoothing were suggested to improve the oxide film uniformity. Post-oxidation high temperature inert Ar annealing was also used to test the thermal stability of oxide films and examine the possible impact of surface conditioning on said stability. Inert annealing at 950°C or 1000°C after oxide growth at 600°C or 850°C, respectively, was found to cause degradation of oxide quality evidenced by an increase in the flat-band voltage ($V_{FB}$) and the calculated net total oxide charge ($Q_{TOT}$). Pre-oxidation (FG)* surface conditioning did

not have any noticeable impact on the $Q_{TOT}$ values before or after annealing. Interfacial rearrangement or viscous oxide flow were suggested as possible factors contributing to the oxide charge increase during annealing.

Non-contact electrical evaluation of SiC surfaces after variations of (FG)* afterglow and other treatments were presented in chapter 4. C-KM measurements were accomplished by deposition of a large pulse of majority charge (depleting the semiconductor) and subsequent monitoring of the $V_{CPD}$ transient. The observed $V_{CPD}$ decay after depletion charging was associated with a decay of the surface potential barrier ($V_{SB}$). Depletion surface barrier decay was attributed to a charge compensation mechanism, suggested to consist primarily of majority carrier emission from traps in the surface region and recombination with dopant ions in the space-charge region deeper in the crystal. The electric field resulting from surface corona charging was expected to assist in the carrier emission and transport processes. The charge compensation mechanism involved a net transport of majority charge away from the surface and into the semiconductor, with corresponding compensation of surface corona charge and decreases in depletion region width and surface barrier height. The observed rate of $V_{SB}$ decay was taken as a measure of surface charge-emitting defect concentrations. Also, the standard deviation of decay behavior averaged from multiple wafer sites was used as a measure of uniformity of surface condition.

Surface conditioning in $(N_2{:}H_2)$* afterglow was determined to result in the lowest rates of $V_{SB}$ decay and least deviation of decay behavior across the wafer, when compared to other treatments including RCA clean, $N_2{:}O_2$ thermal treatment, pure $(N_2)$* afterglow, and $(N_2{:}H_2)$* afterglow followed by DI water rinse, although the latter two were only

slightly worse than the (FG)* treatment. Thus, among the various treatments considered, (FG)* afterglow was concluded to achieve the lowest concentrations of surface charge-compensating defects and highest uniformity of surface condition. Various treatment times ranging 2.5–20 min. of (FG)* afterglow were investigated, revealing a trend of decreasing $V_{SB}$ decay rate and improved uniformity with increasing treatment time. The longest treatment time of 20 min. yielded the lowest levels of surface charge-emitting defects and best uniformity of surface condition. Various (FG)* afterglow treatment temperatures were also investigated. A temperature threshold of conditioning effects was observed, with surfaces treated at 400–500°C demonstrating high rates of $V_{SB}$ decay, and treatments at higher temperatures 600–800°C exhibiting very low decay rates and improved uniformity. Thus a (FG)* treatment temperature 600°C or above was concluded to be necessary to achieve effective conditioning and surface passivation. The state of the SiC surface achieved during (FG)* afterglow conditioning proved to be stable and resilient when exposed to a variety of post-treatment stresses, including temporal, thermal, electrical, and environmental. The effective passivation of surface charge-emitting traps and improved uniformity of surface condition accomplished by (FG)* afterglow treatment were suggested to contribute to the oxide growth rate increase and greater film uniformity observed during subsequent SiC oxidation (chapter 3).

X-ray photoelectron spectroscopy analysis of SiC surfaces was performed to evaluate the impact of (FG)* afterglow conditioning on surface chemistry. The XPS results of chapter 5 compared 4H-SiC surface chemistry after RCA clean or (FG)* afterglow treatment. Surfaces were measured as-received and after sputtering estimated to remove 4 Å of material. Prominent binding energy peaks of Si 2p, C 1s, N 1s, and O

1s core levels were identified and atomic percents were computed. There was no indication of nitrogen on the RCA cleaned sample, while a small N 1s peak was evident on the (FG)*-treated surface which implied nitrogen incorporation during (FG)* afterglow conditioning. The N 1s peak was reduced but still present after sputtering of the (FG)*-treated surface. Oxygen was present after both treatments, attributed to native oxide and contaminant oxygen adsorption during post-treatment air exposure. A higher atomic percent of oxygen was found on the (FG)*-treated surface, presumably due to wafer unloading at 600°C following afterglow conditioning and increased oxygen adsorption to the heated surfaces in air. The C/Si ratio, computed from atomic percents of C 1s and Si 2p peaks, demonstrated a significant decrease on the (FG)*-conditioned surface compared to the RCA clean. The lower C/Si was linked to the removal of carbon resulting in a Si-rich surface region during afterglow conditioning. This silicon enrichment was suggested to be an important contributor to the increased oxide growth rate observed after (FG)* surface conditioning in chapter 3. Furthermore, the removal of C-related defects combined with possible nitrogen passivation of defects were consistent with the reduction of surface defect concentrations achieved during (FG)* afterglow conditioning in chapter 4.

The formation of thermally grown oxide films on 4H-SiC at low growth temperatures of 600–850°C was a unique contribution of this work. This was accomplished only by the use of afterglow chemistry, and would have been impossible using a conventional atmospheric oxidation approach. Also, this work was the first to develop an afterglow surface conditioning process on 4H-SiC specifically to improve subsequent thermal oxidation. This novel contribution was augmented by the

demonstration of the passivating nature of the afterglow conditioning process with respect to depletion charge compensation in 4H-SiC material.

## 6.2. Future work

There exist numerous possibilites for directions of future investigation based on this work. All oxidation experiments presented in this work involved an RCA pre-furnace clean with an optional afterglow surface conditioning step using baseline parameters of 20 min. (FG)* at 600°C. Additional oxidations could be performed using pre-oxidation surface treatments with variations in media, temperature, and time, similar to those of chapter 4.

The standard oxidative media used in this work was ($O_2$:$N_2O$:FG)* 3:0.23:0.5 afterglow. Experiments using ($O_2$:$N_2O$)* with varying amounts of FG would help in illuminating the role of FG during oxidation, and how that depends on starting surface condition.

Further experimentation is required to improve the thermal stability of afterglow oxide thin films on 4H-SiC. The flatband shifting and oxide net charge increase observed during high temperature inert annealing in chapter 3 require improvement if oxide quality is to be stable during post-oxidation thermal processing.

In addition to C-KM capacitance characterization, oxide films could also be analyzed by interpreting the depletion voltage transient decay behavior, analogous to the measurements on surfaces in chapter 4. Changes in the charge transfer process could be correlated with initial surface condition and oxidation parameters.

XPS analysis presented in this work was taken from SiC surfaces after RCA clean or (FG)* afterglow with the baseline treatment parameters of 20 min. exposure at 600°C.

XPS measurements of other surface conditions (media, temperature, time, etc.) would yield additional information regarding the dependence of surface chemistry on treatment variations.

The majority of depletion voltage transients presented in this work incorporated a consistent charge pulse size of $2.4\times10^{-7}$ C cm$^{-2}$ followed by surface barrier monitoring. Further investigation might include exploration of the V-Q relationship, using corona charge pulses of various sizes to characterize the response of surface barrier decay behavior.

Afterglow conditioning of 4H-SiC was shown to prepare a stable and passivated surface with reduced defects and contaminants and greater uniformity. Deposition of alternative dielectric films on such conditioned surfaces could lead to achieving an improvement in interface quality compared to thermally grown oxides on 4H-SiC.

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